PDP TELEVISION

SERVICE MANUAL

MODEL NO. PT4206

Please read this manual carefully before service.

CONTENTS

Part :PP06 Chassis Features and CBU Contents

1.1□PP06 Chassis Technical Specifications□

1.1.1 PT4206 Panel Datas

PT4206 is the most typical model using PP06 chassis; therefore we take PT4206 as an example.

PDP Panel Resolution	852×3(RGB)×480
Colors	16,777,216
Dot Pitch	1.095mm(H)×1.110mm(V)
Brightness	High brightness
Contrast	High contrast
Lifespan of Panel	20000 Hours
Viewing Angle	U/D□160 / L/R□160
Response Time	933mm□H□×533mm(V)

Remarks: Brightness and contrast may vary because of different panels being used. PT4206 mainly uses SAMSUNG SDI panel model S42SD-YD04 or S42SD-YD05

1.1.2 Specification Sheet

PC	Recommended Input Format	640ў 480/60Hz 800ў 600/60Hz
	Unsupportable Input Format Indication	Yes
	Color Temp. Adjust.	Yes
	Quick Plug-In & Use	Yes
	Picture Location Adjust.	Yes
HD Signal J PbPrJ ©	Compatible with	480Pў 576Pў 720P ў 1080i
HD Signal J DVIJ ©	Compatible with	480Pў 576Pў 720P ўў 1080i and HDTV
Video J Including S-VideoJ ©	Picture System	PAL/NTSC/SECAM
	Sound System	D/Kў ў B/Gў ў M
	Digital Comb Filter	Yes
	3D Comb FilterJ NTSCJ ©	Yes
	Movement Compensation Function	Yes
Audio	Output Voltage	2ў 5W
	Audio Effect	WOW
	NICAM/IGR	Yes
	Video/YpbPr Audio Input	Audio L/R
	PC/DVI Audio Input	Audio L/R
Input Voltage	220V~, 50Hz	
Rating Consumption	Ë 400W	
Standby Consumption	Ë 3W	

1.2□Main Features□

1.2.1 Terminals

RF Input	1□Rear□
S Terminal Input	1□Rear□

A/V Input	RCA□1□Rear□
YCbCr	RCA□1□Rear□
DTV YPbPr	RCA□1□Rear□
VGA/SVGA Input	Hi-Density D-SUB 15 pin connector□1□Rear□
DVI Input	1 Rear
A/V Output	RCA□ Rear

Remarks: PT4206 is equipped with a service terminal, which service people can connect with PC RS232 terminal to upgrade the software.

1.2.2 Working Condition Requirement:

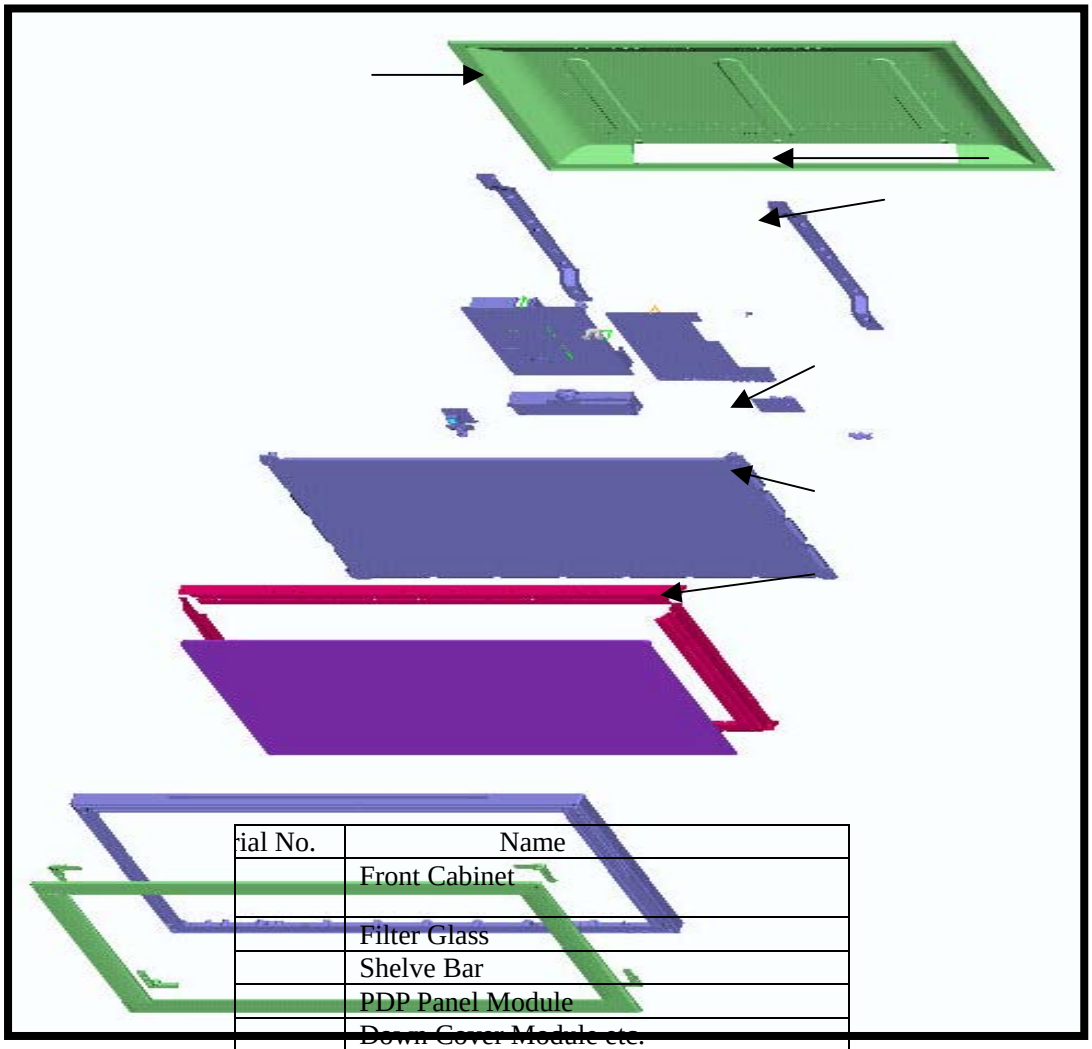
Working Condition Requirement	Temperature	0□□40
	Humidity	20□□70□
	Altitude	0□2000m

1.2.3 Others

Tuning System	FS Tuning□236 Programs
NICAM Demodulation	Yes
Audio Effect Process	AV stereo□SRS WOW□5 Bands Equalizer
Picture Freeze	TV/AV/S-VIDEO/YcbCr Only
On Screen Display	Chinese/English, Menu Location movable by user.
Blue Background without Signal	Yes
Power Saving	When TV is connected with PC input, while there is no signal from PC, after 60 seconds, TV will be automatically off and enter into Power Saving Mode. Press any key on TV or R/C, or there is signal from PC again, TV will be switched on automatically.
Pixel Movement	When this function is on, pictures will move on regularly to protect the screen.
White Screen Display	When this function is on, the screen will be completely white to clear up slight shadows□please see the instruction manual for more details□
Home/Commercial Mode Optional	Users can choose between 15 minutes auto-off without signal or 3 hours auto-off without operation □ please see the instruction manual for more details□

1.3□CBU Content

1.3.1 PDP Inside Drawing:

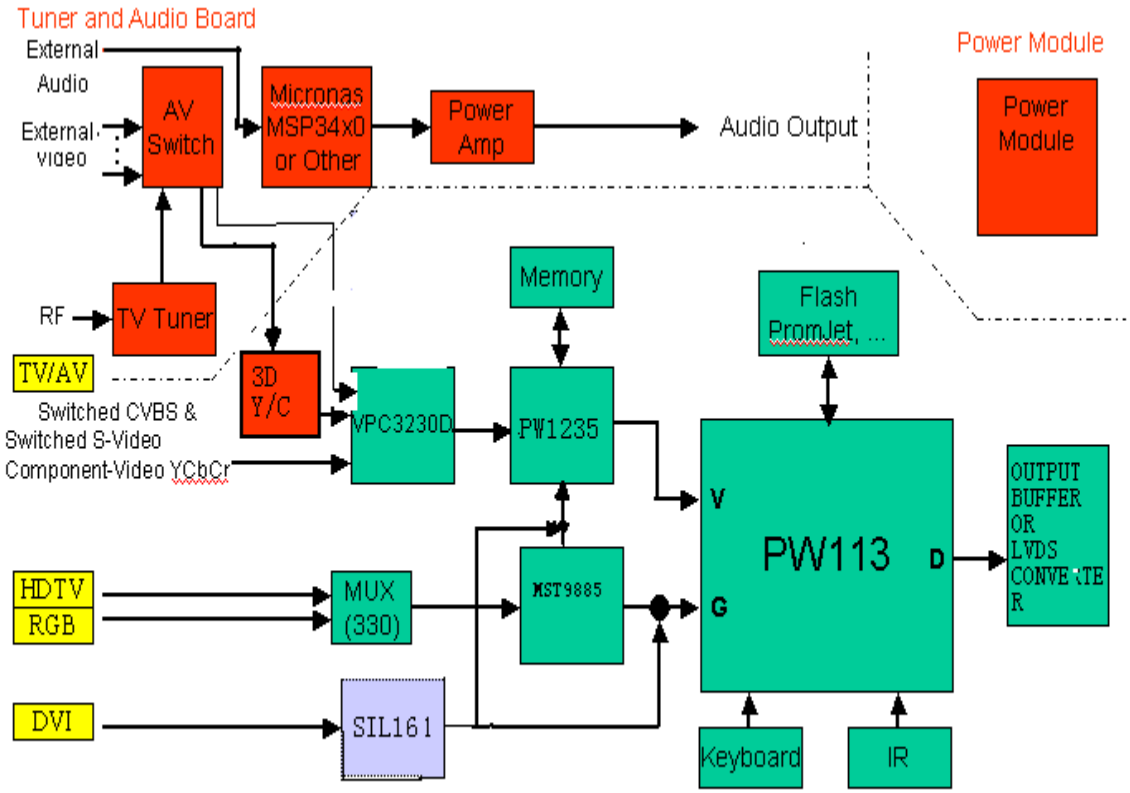


rial No.	Name
	Front Cabinet
	Filter Glass
	Shelve Bar
	PDP Panel Module
	Down Cover Module etc.
	Back Cabinet

Remarks: This drawing is for references only, please see the main assembly diagram and wire-connecting diagram for details.

1.3.2 Circuit Content□

The main content of PP06 circuit include: Power Regulating Circuit, RF Circuit, VGA, Analog Video, Digital Video Signal Processing Circuit, System Control Circuit, Button Control Circuit. Reference drawing as below:



Part :Introduction on Circuit Functions of PT4206

2.1 Changhong PDP TV PT4206 main IC functions□

NO.	NAME	TYPE	Function
1	N901	TDQ-6F7-FM2W	Unify tuner
2	N601	MSP3410G-C12-100	Sound disposal
3	U705	TA2024	sound amplifier
4	U701	uPD64083GF-3BA	NTSC 3D comb filter
5	N902	TEA6425D	AV video switch
6	U1	VPC3230D-QA-B3	Digital video disposal
7	U6	MST9885	A/D converter
8	U11	SiI161BCT100	DVI signal disposal
9	U16	PW113-20Q	Format transform and MCU
10	U17	AM29LV800BT-90	FLASH ROM
11	U22	DS90C383AMTD	Difference transmit
12	U20	ST232CD	RS-232 signal disposal
13	U7	24LC21A/SN	E²PROM□display parameter information□
14	U9/U13	SN74LVC126AD	Suffer amplifier
15	U71	74LV32D	Sync. face lifting enlarge
16	U8	24LC21A/SN	E²PROM□DVI parameter information□
17	U19	24LC32A/SN	E²PROM□user control information□
18	U4	IS42S16400(A)-7T	SDRAM
19	U5	PI5V330(Q)	RGB/YpbPr switch
20	U3	PW1235	IP transform and picture improve

2.2□Changhong PDP TV PT4206 main IC functions introduction□

2.2.1 A/D converter MST9885 General□

The MST9885 is a fully integrated analog interface for digitizing high-resolution RGB graphics signals from PCs and workstations. With a sampling rate capability of up to 140 MHz, it can accurately support display resolutions up to 1280x1024 (SXGA) at 75 Hz. The clamped input circuits provide sufficient bandwidth to accurately digitize each pixel.

The MST9885B provides a high performance highly integrated solution to support the digitization process, including the ADCs, a voltage reference, a PLL to generate the pixel sampling clock from HSYNC, clamping
circuits, and programmable offset and gain circuits to provide brightness and contrast controls.

When the COAST signal is asserted, the PLL will maintain its output frequency when HSYNC pulses are absent, such as during the VSYNC period in some systems.

A 32-step programmable phase adjustment control (0-360 deg) is provided for the pixel sampling clock to adjust for the difference between the HSYNC edge and RGB pixel edge timing.

The MST9885B can send output data through one 24-bit port at the pixel clock rate.

The MST9885B can also support R, G, B to Y, U, V conversion.

The MST9885B has internal programmable pattern generator for testing.

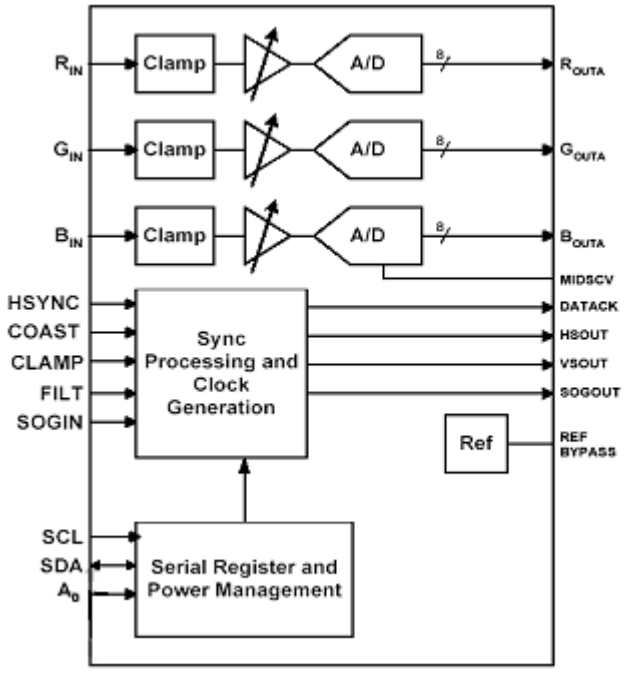
The MST9885B can accept either standard TTL, CMOS levels or sawtooth vertical deflection signals for VSYNC input.

MST9885 Pin Function Descriptions□

Pin(s)	name	Function
70□77	RED0□RED7	Red output data
2□9	GREEN0 □	Green output data

	GREEN7	
12□19	BLUE0□BLUE7	Blue output data
67	DATACK	Output data clock
66	HSOUT	HSYNC output
65	SOGOUT	Sync-on- Green Slicer output
64	VSOUT	VSYNC output
37	MIDSCV	Internal mid-scale voltage bypass
58	REFBYP	Internal reference bypass
31	VSYNC	Vertical SYNC input
30	HSYNC	Horizontal SYNC input
43	BAIN	Blue analog input
49	SOGIN	Sync-on- Green analog input
48	GAIN	Green analog input
54	RAIN	Red analog input
29	COAST	Hold PLL frequency and do not track HSYNC
38	CLAMP	External clamp input(we connect it to ground □
55	A0	Serial interface address pin
56	SCL	I^2C bus□clock□
57	SDA	I^2C bus□data□
33	FILT	PLL connect to external filter
26□27□39□ 42□45□46□ 51□52□59□ 62	AVDD	Analog power
11□22□23□ 69□78□79	V33	Digital output power
34□35	PVDD	PLL power
1□10□20□21□ 24□25□28□ 32□36□40□ 41□44□47□ 50□53□60□ 61□63□68□ 80	GND	ground

MST9885 Block Diagram□

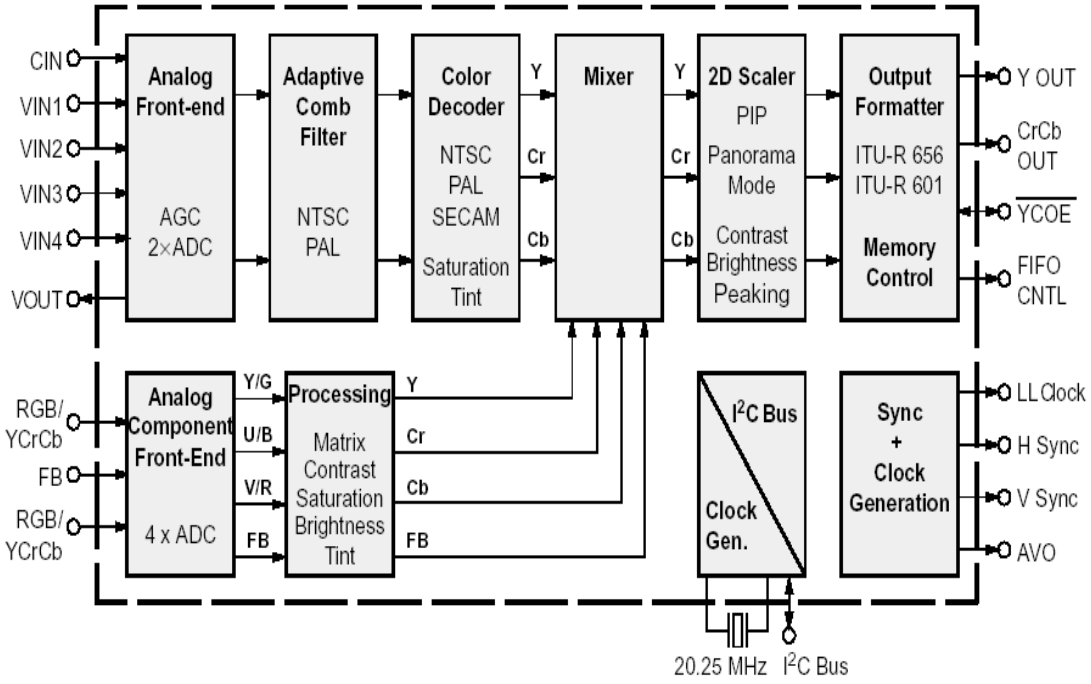


2.2.2□VPC3230 General□

VPC3230 Pin Function Descriptions□

Pin No.	Pin Name	Short Description
1□3	R1G1B1IN	RGB Analog Component Input 1
4□6	R2G2B2IN	RGB Analog Component Input 2
7□64□30□ 11□12□25□ 35□65□77□ 46□51□68□ 80	GND	GND
8	NC	NC
9	VSUPCAP	Supply Voltage, Digital Decoupling Circuitry
10□29□36□ 45□52	V33	Supply Voltage, Digital Circuitry
59□69□76	AVCC	Analog Voltage
13	SCL	I^2C Bus Clock
14	SDA	I^2C Bus Data
15	RESQ	Reset Input
16	TEST	Test Pin
17	VGAV	VGAV Input
18	YCOEQ	Y/C Output Enable Input
19□23	FFIE	NC
24	CLK20	Main Clock Output
27	LLC2	Clock Output
28	LLC1	NC
31□34 37□40	Y0□Y7	YUV signal output (Digital ITU-R656 format)
41□44 47□50	C0□C7	Digital chromatic signal output
53	INTLC	Interlace scan control output (0-odd,1-even)
54	AVO	Active Video Output
55	FSY/HC	NC
56	MSY/HS	Horizontal Sync Pulse output
57	VS	Vertical Sync Pulse
58	FPDAT	NC
60	CLK5	5 MHz Clock Output
61	NC	NC
62	XTAL1	20.25M Analog Crystal Input
63	XTAL2	20.25M Analog Crystal Output
66	VRT	Reference Voltage Top, Analog
67	I^2CSEL	I^2C Bus Address Select
70	VOUT	Analog Video Output
71	CIN	Chroma / Analog Video 5 Input
72	VIN1	Video 1 Analog Input
73	VIN2	Video 2 Analog Input
74	VIN3	Video 3 Analog Input
78	VREF	Reference Voltage Top
79	FB1IN	Fast Blank Input

VPC323Ø Block Diagram□



2.2.3□PW113 General□

The PW113 integrates an industry-leading scaler, an advanced OSD engine, a flexible input port system, system memory, and a powerful 80186-based □horizontal and vertical image scaler swith intelligent Auto Image Optimization circuitry□The Image Processor supports NTSC or PAL video data with a 4:3 aspect ratio and 16:9 aspect ratio sources, such as DVD or HDTV. Video Input formats can be in either YUV4:4:4 (24 bit) or YUV4:2:2 (16 bit) input modes□The PW113 uses an integrated PLL to synchronize the display interface timing to the input timing□An integrated OSD controller supports sophisticated bit-mapped based OSDs The OSD controller supports transparent, translucent, and fade-in/ fade-out functions.

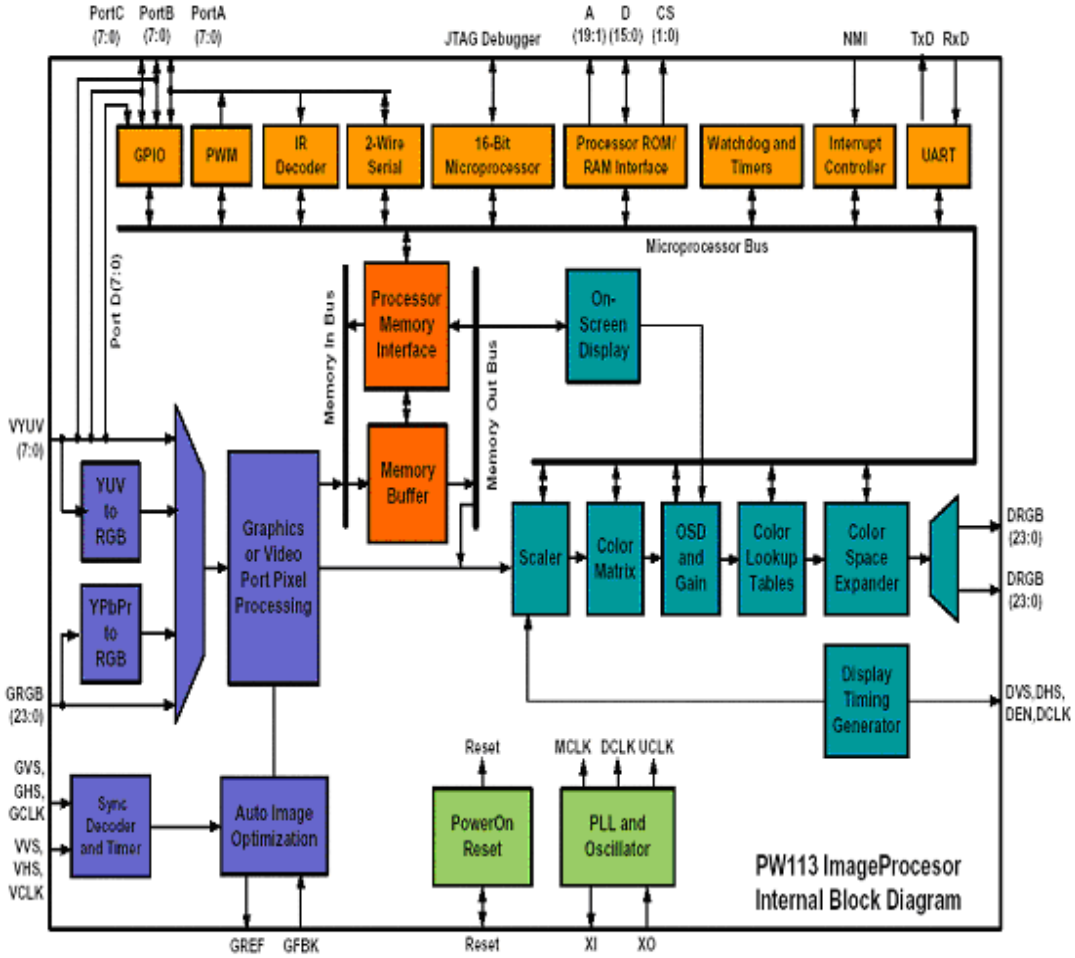
Pin Function Descriptions□

Pin(s)	name	Function
Video Port Pin Descriptions		
71	VCLK	VPort Pixel Clock input
74	VVS	VPort Vertical Sync input
75	VHS	VPort Horizontal Sync input
69	VFIELD	VGPort Field Input
70	VPEN	VPort Pixel Enable
47□56	YUV0□YUV7	VGPort ITUR656 Pixel Data.□I/O port□ We use □ 47 MUTE mute control □ 48 PW1230E PW1235output enable□49 VGASEL VGA/YpbPr select□50 S1 sound system control□51 DVIPD DVI interface standby□ 54 STANDBY power standby control□56 RST1 peripheral IC reset
Graphics Port Pin Descriptions		
31	GCLK	GPort Pixel Clock input
32	GVS	GPort Vertical Sync input
33	GHSSOG	GPort Horizontal Sync/GPort Sync- on-Green input
34	GPEN	GPort Pixel Enable input

35	GFBK	GPort PLL Feedback / Line Advance Input
20□27	GRE0□GRE7	GPort Red Pixel Data input
10□15□18□19	GGE0 □ GGE7	GPort Green Pixel Data input
2□9	GBE0□GBE7	GPort Blue Pixel Data input
Display/Graphics Port Pin Descriptions		
129□136	DGR0□DGR7	DGPort Red Pixel Data(odd outputs)
119□122□ 125□128	DGG0□DGG7	DGPort Green Pixel Data(odd outputs)
111□118	DGB0□DGB7	DGPort Blue Pixel Data(odd outputs)
Display Port Pin Descriptions		
106	DCLK	DPort Pixel Clock output
108	DVS	DPort Vertical Sync output
109	DHS	DPort Horizontal Sync output
110	DEN	DPort Pixel Enable output
96□103	DR0□DR7	DPort Red Pixel Data(even outputs)
88□95	DR0□DR7	DPort Green Pixel Data(even outputs)
76□83	DB0□DB7	DPort Blue Pixel Data(even outputs)
Microprocessor Interface Pin Descriptions		
194	WR	Write Enable low indicates a write to external RAM or other devices
195	RD	Read Enable low indicates a read to external RAM or other devices
196	ROMOE	ROM Output Enable low output indi cates a read from external ROM.
197	ROMWE	ROM Write Enable low indicates a write to external ROM.
198	CS0	Chip select signal
199	CS1	Chip select signal
193	NMI	Non-maskable Interrupt
164□173□ 184□187□ 192	A1□A19	Microprocessor address bus output bits
148□163	D0□D15	Microprocessor 16-bit bidirectional data bus
Peripheral Interface Pin Descriptions		
207	PORTA0	DISPEN signal output(PDP display control)
206	PORTA1	READY signal input□PDP display ready□
205	PORTA2	SDA
204	PORTA3	SCL
203	PORTA4	IR receive signal input
201	PORTA6	DVI digital interface select control
203	PORTA4	IR receive signal input
57□58□60□ 64	PORTB0 □ PORTB7	Key control input
39	PORTC0	MA-EN enable control
40	PORTC1	480ISEL 480I anti-copy control
41	PORTC2	RST-1235 PW1235 reset
42	PORTC3	DIGSEL DVI digital interface select
43	PORTC4	LVDSON LVDS enable control
44	PORTC5	S0 sound system control
45□46	PORTC6 □ PORTC7	LED control
67	RXD	Serial Receive Data
68	TXD	Serial Transmit Data
Miscellaneous Pin Descriptions		
142	TEST	Test mode enable
139	RESET	Bidirectional reset pin

169	XI	Crystal input
170	XO	Crystal output
Power and Ground Pin Descriptions		
16□37□65□84□137□185	VDD1	1.8V digital core power.
17□38□66□85□138□186	VSS	Digital core ground
29□52□72□86□104□123□140□171□208	VDDQ3	3.3V digital I/O power.
1□30□53□73□87□105□124□141□172	VSSQ	Digital I/O ground.
165	VDDPA2	1.8V analog clock generator power.
166	VSSPA2	Clock generator analog ground.
167	VDDPA1	1.8V analog clock generator power.
168	VSSPA1	Clock generator analog ground.

PW113 Block Diagram



2.2.4□PW1235 General

PW1235 supports standard digital video signal □ incorporates deinterlacing□

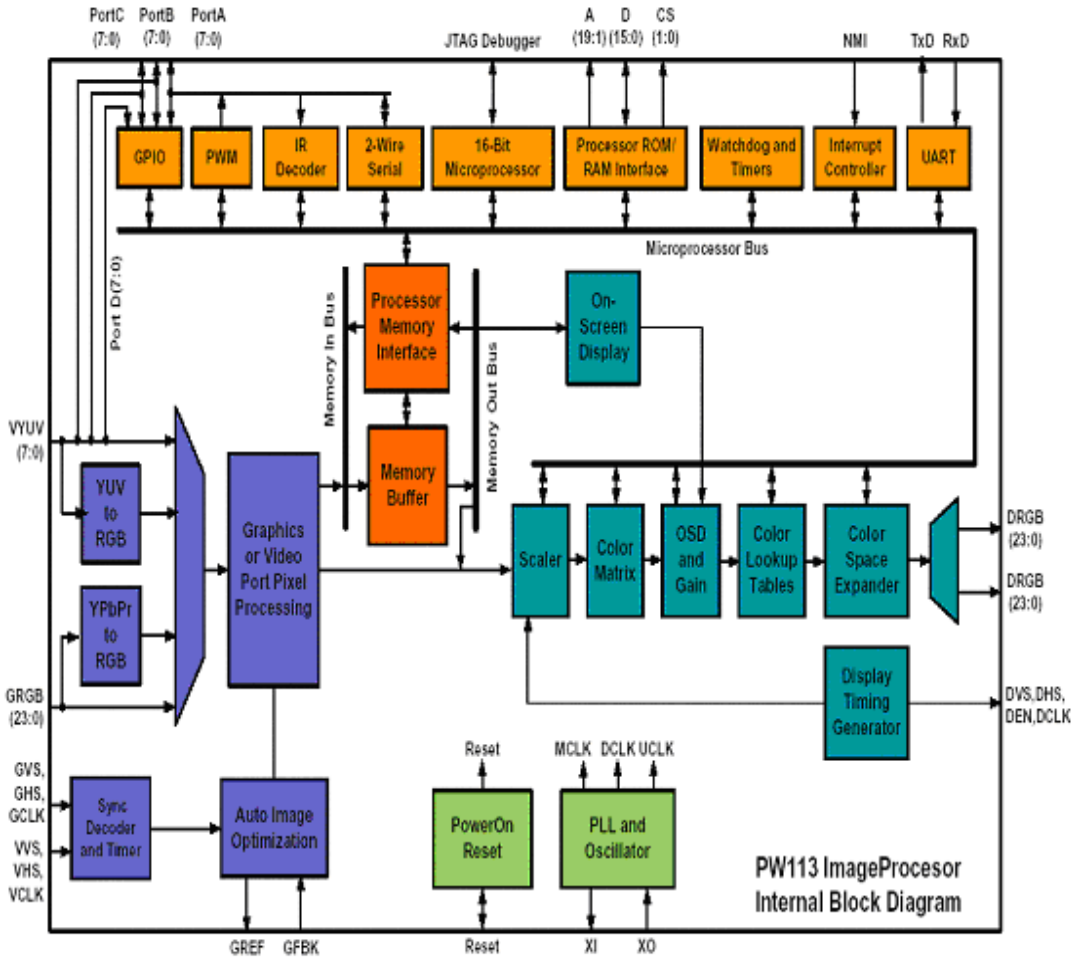
scaling .the PW1235 is able to effectively deinterlace video input by creating motion vectors that follow frame-to-frame movement, and provide clear, progressive output in both analog and digital formats. The PW1235 integrates input interface□MEMORY control circuit□picture improve□ output interface circuit□I^2C bus interface and so on□all the function are controlled by I^2C bus□

Pin Function Descriptions□

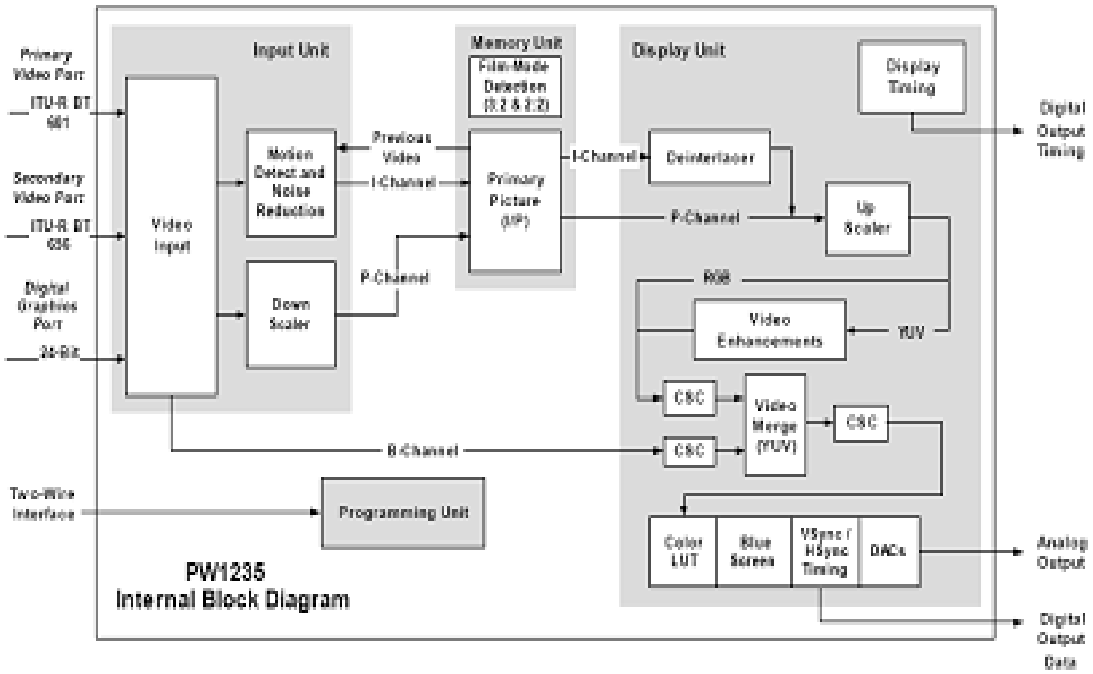
Pin(s)	Name	Function
Video Port Pin Descriptions		
27	PVVS	Primary Video (PV) Port vertical sync input.
28	PVHS	Port horizontal sync input
25	PVCLK	Port pixel clock input
26	CREF	Video input clock reference
12	SVVS	Port (ITU-R BT656 format) vertical sync input
11	SVHS	Port (ITU-R BT656 format) horizontal sync input
13	SVCLK	Port (ITU-R BT656 format) pixel clock input
30□33□35□38	VR0□VR7	Video port red data input
15□18□20□23	VG0□VG7	Video port green data input
1□4□6□9	VB0□VB7	Video port blue data input
Digital/Graphics (DG) Port Pins		
68	DGCLK	Digital/Graphics (DG) port pixel clock
67	DGVS	Digital/Graphics (DG) port vertical sync.
66	DGHS	Digital/Graphics (DG) port horizontal sync
91□92□94□95□ 97□100	DGR0 □ DGR7	Digital/Graphics (DG) port red data
81□84□86□89	DGG0 □ DGG7	Digital/Graphics (DG) port green data.
70 □ 73,75 □ 76 □ 78□79	DGB0 □ DGB7	Digital/Graphics (DG) port blue data
Analog Display Port Pin Descriptions		
156	ADR	Analog display port red (V/Pr) data
153	ADG	Analog display port green (Y/Y) data
150	ADB	Analog display port blue (U/Pb) data
161	VREFIN	Reference voltage input.
162	VREFOUT	Reference voltage output.
159	RSET	Full-Scale adjust resistor
160	COMP	Compensation pin
Digital Display Output Port Pin Descriptions		
102	DCLK	Digital display output port pixel clock
103	DVS	Digital display output port vertical sync
104	DHS	Digital display output port horizontal sync.
108	DENR	Display pixel enable red/Vertical blanking period (VBLANK)
106	DENG	Display pixel enable green
107	DENB	Display pixel enable blue/Horizontal blanking period (HBLANK)
145	DEN	Digital display output port output enable
132 □ 133 □ 135 □ 136 □ 138 □ 139 □ 141□142	DR0□DR7	Digital display output port red data
121 □ 122 □ 124 □ 125 □ 127□130	DG0□DG7	Digital display output port green data.
110 □ 111 □ 113 □ 114 □	DB0□DB7	Digital display output port blue data.

116□119		
Memory Pin Descriptions		
229	MCLK	SDRAM clock
223	MCLKFB	SDRAM clock feedback
225	MRAS	SDRAM row address strobe
226	MCAS	SDRAM column address strobe
227	MWE	SDRAM write enable
213□210□207□204□ 203□206□209□211□ 214□217□215□220□ 221□218	MA0 □ MA13	SDRAM address bus
255□252□248□245□ 242□239□236□232□ 231□234□238□241□ 244□247□250□254	MD0 □ MD15	SDRAM data bus
Host Interface Pin Descriptions		
47	2WDAT	SDA
45	2WCLK	SCL
43	2WA1	Programmable two-wire serial bus address bit 1
44	2WA2	Programmable two-wire serial bus address bit 2
178□179□181□186	MCUD0 □ MCUD7	MCU data bus
168□170□172□ 174□176□177	PORTB1	MCU address bus
190	MCUCS	Chip select
191	MCUWR	MCUR/W signal
192	MCUCMD	MCU command signal
188	MCURDY	MCU Ready signal
Miscellaneous Pin Descriptions		
56	TEST	Test mode
144	TESTCLK	Used for testing, can be used to supply display clock
55	RESETn	Hardware asynchronous reset.
40	XTALI	Crystal oscillator input
41	XTALO	Crystal oscillator output
146	CGMS	CGMS Enable
201	MVE	Macrovision write protected enable
62, 63, 194,195	NC	
System Power Pin Descriptions		
5, 34, 93, 123,140, 175,205, 235	VDD	Digital core power (2.5V).
19, 49, 77, 112, 134, 187, 219, 251	VSS	Digital core ground.
14, 29, 42, 54, 64, 69, 80, 90, 101, 109, 120, 131, 143, 165, 180, 200, 208, 216, 224, 230, 237, 243, 249, 256	PVDD	Digital I/O power (3.3V).
10, 24, 39, 46, 57, 65, 74, 85, 96, 105, 115, 126, 137, 147, 171, 189, 193, 202, 212, 222, 228, 233, 240, 246, 253	PVSS	Ground.
60	MPAVDD	Memory PLL analog power 2.5V.

61	MPAVSS	Memory PLL analog ground.
58	MPDVDD	Memory PLL guard ring / digital power 2.5V.
59	MPDVSS	Memory PLL guard ring / digital ground.
197	DPAVDD	Display PLL analog power 2.5V.
196	DPAVSS	Display PLL analog ground.
199	DPDVDD	Display PLL digital power 2.5V.
198	DPDVSS	Display PLL digital ground.
157	AVD33R	Analog power (+3.3V) for R (V/Pr) channel.
154	AVD33G	Analog power (+3.3V) for G (Y/Y) channel.
151	AVD33B	Analog power (+3.3V) for B (U/Pb) channel.
158	AVS33R	Analog ground for R (V/Pr) channel.
155	AVS33G	Analog ground for G (Y/Y) channel.
152	AVS33B	Analog ground for B (U/Pb) channel.
163	ADAVDD	Analog power supply (+2.5V) for the analog display port.
164	ADAVSS	Analog ground for the analog display port.
149	ADDVDD	Digital power supply (+2.5V) for the analog display port.
148	ADDVSS	Digital ground for the analog display port.
166	ADGVDD	Guard ring power for the analog display port.
167	ADGVSS	Guard ring ground for the analog display port.



PW1235 Block Diagram □



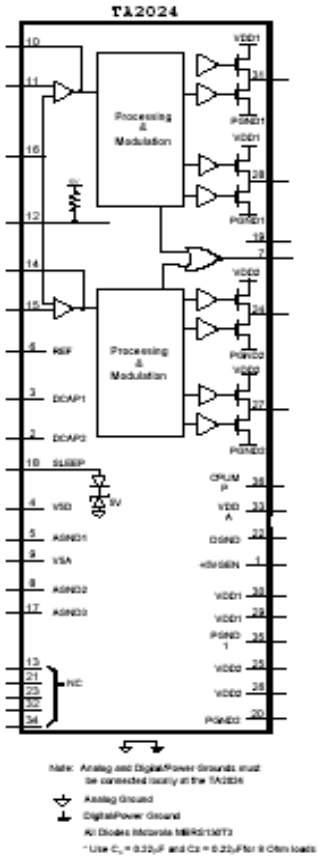
2.2.5 TA2024 general:

The TA2024 is a 10W/ch continuous average two-channel Class-T Digital Audio Power Amplifier IC using Tripath's proprietary Digital Power Processing™ technology. Class-T amplifiers offer both the audio fidelity of Class-AB and the power efficiency of Class-D amplifiers.

Pin Function Descriptions:

Pin(s)	Name	Function
2, 3	DCAP2, DCAP1	Charge pump switching pins
4, 9	V5D, V5A	Digital 5VDC, Analog 5VDC
5, 8, 17	AGND1, AGND2, AGND3	Analog Ground
6	REF	Internal reference voltage
7	OVERLOADB	A logic low output indicates the input signal has overloaded the amplifier
10 14	OAOUT1, OAOUT2	Input stage output pins.
11, 15	INV1, INV2	Single-ended inputs
12	MUTE	Mute control
16	BIASCAP	Input stage bias voltage
18	SLEEP	Sleep mode control
19	FAULT	A logic high output indicates thermal overload
20, 35	PGND2, PGND1	Power Grounds (high current)
22	DGND	Digital Ground
24, 27; 31, 28	OUTP2 & OUTM2; OUTP1 & OUTM1	Bridged outputs
25, 26, 29, 30	VDD2, VDD2 VDD1, VDD1	Supply pins for high current H-bridges, nominally 12VDC.
13, 21, 23, 32, 34	NC	Not connected
33	VDDA	Analog 12VDC
36	CPUMP	Charge pump output
1	5VGEN	Regulated 5VDC source used to supply power to the input section (pins 4 and 9).

TA2024 Block Diagram□



2.2.6□DS90CF383A General

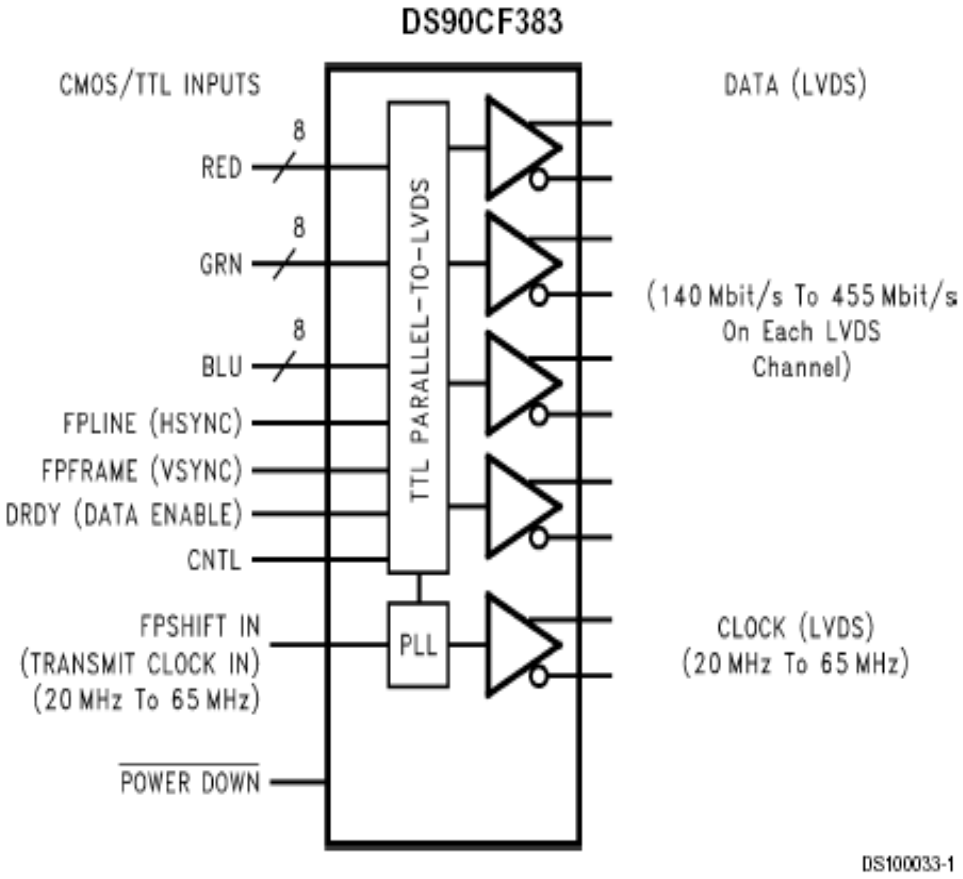
The DS90C383A/DS90CF383A transmitter converts 28 bits of CMOS/TTL data into four LVDS (Low Voltage Differential Signaling) data streams. A phase-locked transmit clock is transmitted in parallel with the data streams over a fifth LVDS link. Every cycle of the transmit clock 28 bits of input data are sampled and transmitted. At a transmit clock frequency of 65 MHz, 24 bits of RGB data and 3 bits of LCD timing and control data (FPLINE, FPFRAME, DRDY) are transmitted at a rate of 455 Mbps per LVDS data channel. Using a 65 MHz clock, the data throughput is 227 Mbytes/
sec. The DS90C383A transmitter can be programmed for Rising edge strobe or Falling edge strobe through a dedicated pin. The DS90CF383A is fixed as a Falling edge strobe transmitter.

Pin Function Descriptions□

Pin(s)	Name	Function
1,9,17,26,34 44	VCC	Power supply
5,13,21,29,53 33,35,36,43,49	GND	Ground
2,3,50,51,52 54,55,56	DRE0□DRE7	8bit red data input
4,6,7,11,12,14 8,10	DGE0□DGE7	8bit green data input
15,19,20,22 23,24,8,16	DBE0□DBE7	8bit blue data input

27	HSYNC	Horizontal Sync input
28	VSYNC	Vertical Sync input
30	DE	pixel display enable
31	TXCLK IN	pixel display clock input
32	$\overline{PWRDWN}$	LVDS control
37,38,41,42 45,46,47,48	TXOUT+ TXOUT-	4 channels LVDS data signal output
39,40	TXCLKOUT+ TXCLKOUT-	1 channel LVDS clock signal output

DS90CF383 Block Diagram□



Order Number DS90CF383MTD
See NS Package Number MTD56

2.2.7□DVI Digital Receiver SiI161B

General□

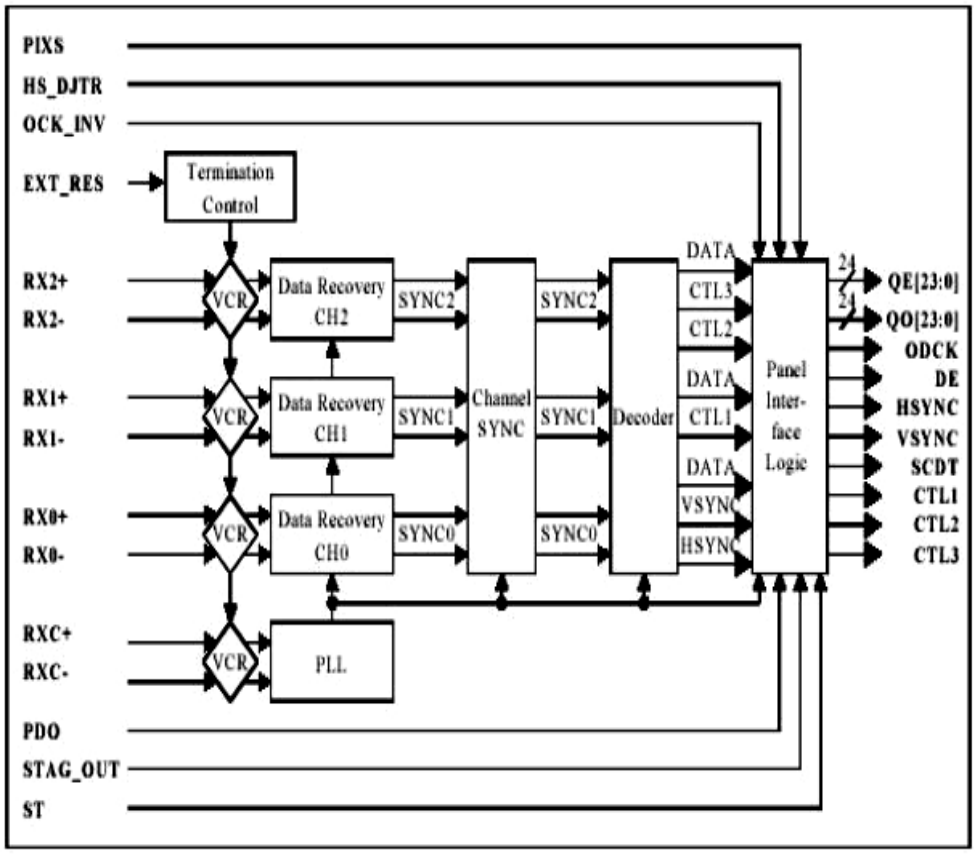
The Sil161B receiver uses Panel Link Digital technology to support high-resolution displays up to UXGA. The Sil161B receiver supports up to true color panels (24 bit/pixel, 16.7M colors) in 1 or 2 pixels/clock mode. In addition, the receiver data output is time staggered to reduce ground bounce that affects EMI. All Panel Link products are designed on a scaleable CMOS architecture. This ensures support for future performance requirements while maintaining the same logical interface. With this scalable architecture, system designers can be assured that the interface will be fixed through a number of technology and performance generations.

Pin Function Descriptions☐

Pin(s)	Name	Function
90	RX0+	TMDS Low Voltage Differential Signal input data pairs
91	RX0-	TMDS Low Voltage Differential Signal input data pairs
85	RX1+	TMDS Low Voltage Differential Signal input data pairs
86	RX1-	TMDS Low Voltage Differential Signal input data pairs
80	RX2+	TMDS Low Voltage Differential Signal input data pairs
81	RX2-	TMDS Low Voltage Differential Signal input data pairs
93	RXC+	TMDS Low Voltage Differential Signal input clock pair.
94	RXC-	TMDS Low Voltage Differential Signal input clock pair.
49 56	QO0 QO7	8bit odd-pixel Blue output
59 66	QO8 QO15	8bit even-pixel Green output
69 75,77	QO16 QO23	8bit odd-pixel Red output
10 17	QE0 QE7	8bit even -pixel Blue output
20 27	QE8 QE15	8bit even -pixel Green output
30 37	QE16 QE23	8bit even -pixel Red output
99	RESERVED	Must be tied HIGH for normal operation.
100	OCK_INV	ODCK Polarity. A LOW level selects normal ODCK output. A HIGH level selects inverted ODCK output.
1	HS_DJTR	This pin enables/disable the HSYNC dejitter function. To enable the HSYNC function this pin should be tied high. To
2	PD	Power Down (active LOW). A HIGH level indicates normal operation. A LOW level indicates power down mode.
3	ST	Output Drive. A HIGH level selects HIGH output drive strength. A LOW level selects LOW output drive strength.
4	PIXS	Pixel Select. A LOW level indicates one pixel (up to 24-bits) per clock mode using QE[23:0]. A HIGH level indicates two pixels (up to 48-bits) per clock mode using QE [23:0] for first pixel and QO[23:0] for second pixel.
7	STAG_OUT	Staggered Output. A HIGH level selects normal simultaneous outputs on all odd and even data lines. A LOW level selects staggered output drive.
8	SCDT	Sync Detect. A HIGH level is outputted when DE is actively toggling indicating that the link is alive. A LOW level is outputted when DE is inactive, indicating the link is down.
9	PDO	Output Driver Power Down (active LOW). A HIGH level indicates normal operation. A LOW level puts all the output drivers only (except SCDT and CTL1) into a high impedance (tri-state) mode.
44	ODCK	Output Data Clock. This output can be inverted using the OCK_INV pin.
46	DE	Output Data Enable.
47	VSYNC	Vertical Sync input control signal.
48	HSYNC	Horizontal Sync input control signal.
18,29,43,57,78	OVCC	Output VCC
19,28,45,58,76	OGND	Output GND
6,38,67	CVCC	Digital Core VCC,
5,39,68	GND	Digital Core GND.
82,84,88,95	DAVCC	Analog VCC

99,83,87,89,92	AGND	Analog VCC
97	PVCC	PLL Analog VCC
98	PGND	PLL Analog GND.
96	EXT-RES	Impedance Matching Control. In the common case of 50Ω transmission line, an external 390Ω resistor must be connected between AVCC and this pin.

SiI161B Block Diagram□



CHAPTER 3 CHANGHONG PDP TELEVISON PT4206

entire signal flow analyse

3.1□Each part signal Disposal Flow general

3.1.1□Analog signal Disposal Flow

3.1.1 .1RF Disposal

TDQ-6F7-FMW2 disposal the RF signal

Pin Function Descriptions□

Pin(s)	Name	Function
1	VT	Analog tune voltage□not use□
2	BTL	+32Vpower
3	BM	+5V power
4	ADD	Ground
5	S0	Color system Switch control
6	S1	Color system Switch control
7	SCL	I^2C bus□clock□
8	SDA	I^2C bus□data□
9	SIF	Second sound IF signal output
10	VIDEO OUT	video signal output
11	VIF	Power supply
12	AUDIO OUT	Sound LF signal output(not use)

First the antenna signal enters the Unify RF TUNER N901, enlarge the RF signal , choose the back track of frequent and mix frequent circuit ,and outputs the IF signal. The video signal from the 9 pin through the video check wave, differs to clap at the same time the Second sound IF signal output.

The frequency synthesizing and tuning needs two power supplies when work normally:+ 32 V tune voltage and + 5 V PLL power supply.

Moreover 5 and 6 pin of N901 switch the Color system , sending out from 44 and 50 pin of PW113.10 pin of N901 outputs video signal ,follows to Q905 ,through the video switch circuit switching with the AV/ S- VIDEO
Input signal ,after them disposal in VPC3230.

3.1.1 .2 SOUND Disposal□

the 9 pin of N901 outputs the second sound IF signal, enlarged by the Q910,following to Q602 and passing C611 to the 67 pin of MSP3410G to carry on SIF demodulation and the NICAM identify the decoding□The sound of PC, DVI, AV, YCbCr, and YPbPr are transited to MSP3440, and then input to the speakers after transits to TA2024 and to the speakers.

.

3.1.1.3 digital signal disposal

In response to input signal of PW113 ,it must convert the input analog video signal, VGA analog signal and DVI signal into digital or video decode output□include three parts□one, VGA or YpbPr (analog signal)is converted the signal into A/D by MST9885□it is 24bit digital tricolor signal□second various video signals□include TV signal□ are disposalled by VPC3230 □then output the signal format ITU-R656 YUV signal□The third part decode DVI1.0 standard digital signal then output 24bitRGB signal□

3.1.1 .4 VGA/YpbPr analog signal disposal□

R, G, B signal From the VGA 1, 2, 3 pin through the static electricity protection circuit switches with video signal from YpbPr input port in PI5V330. After then R□G□B signal(PC source) pass C81□C82□C84 to 54□48□43 pin of MST9885 and A/D converter in it□

Moreover , Vertical , Horizontal sync from the VGA 13,14 pin also send to the synchronous pulse orthopedics circuit after static electricity protect processing. Horizontal sync after face lifting in 74LCX32 sends to the PI5V330 to the switch , and then feedback to the 30 pins of MST9885, By the effect of Horizontal sync , MST9885 creates PLL lock providing the MST9885 work clock. Vertical sync after buffer and enlarge in U71 outputs from the 6 pin of U71, and choices in U9(74 LVC126s).In VGA mode ,the signal to the 31 pin of MST9885, provides a Vertical sync to the MST9885.

The PDP display is the exterior equipments, and need an identify signal to examined by host when host communication. The 24LC21s of U8(EEPROM) saves the hardware concerning display parameter.(install etc. such as the factory, model number, resolution)

MST9885 under the control of PW113 bus, converts the R,G,B input 8 bit digital R,G,B signal. 67 pin outputs pixel clock signal DATACK□The above signal sends to the PW113 and PW1235s at the same time, disposals the format judged by PW113.

3.1.1.4 Analog video signal disposal□

9 pin of N901 outputs video signal passes VN901 and goes to 1 pin of TEA6425D□at the same time 1 channel AV video signal sends to the 8 pin of TEA6425D□and other channel S-video signal (Y□C signal) sends to 6□5 pin of TEA6425D respectively. The three signals switches in the TEA6425D. VIDEO or Y signal outputs toVPC3230D from 17pin□C signal outputs from 18pin□at the same time 19 pin video outputs from19 pin□VPC3230 The signal from TEA6425 after switch and A/D□send to chroma decode circuit ,which can identify PAL/NTSC/SECAM signal automatically □and to each decode after identify. Such as NTSC video after identify □the system switches the TEA6425D channel □sends to NTSC 3D comb filter from 14 pin of TEA6425D. After digital 3D comb filter in uPD64083□ YC signal sends back to 73□71pin of VPC3230D□to AD convertor and saturation control etc. The output digital YUV signal□switches with digital YUV signal after A/D which inputs from 4□5□6pin□and outputs digital YUV signal sends to video disposal□include zoom□contrast□ panorama mode□brightness□gain control tc. After then the signal transforms to from 31□40pin digital YUV signal□4:2:2□(ITU-R656 format)and sends to PW1235 to DEINTERLACE etc□

3.1.1 .5 DVI digital signal disposal□

We use DVI-D interface □

DVI digital signal□4channels DS signal□from DVI jack each send to 90□91□85□86□80□81□93□94pin of SiI161B. By the control of 100□3pin (input bus)□after in SiI161B(VCR□data resume□sync. Head test □ enlarge circuit□decode circuit and logic interface circuit)□it outputs digital R G B signal□which has two mode□one mode when 4 pin of SiI161B is low□ it output 24bit even pixel□when 4pin is high□ it output 48biteven and odd pixel data□we connect 4pin to ground□so each signal from 10□17□20□27□30□37pin outputs R,G,B even pixel data□ switch with 24bit VGA digital signal disposalled by MST9885□and send to PW113 to transform

format□for sure ,the choice is control by PW113□

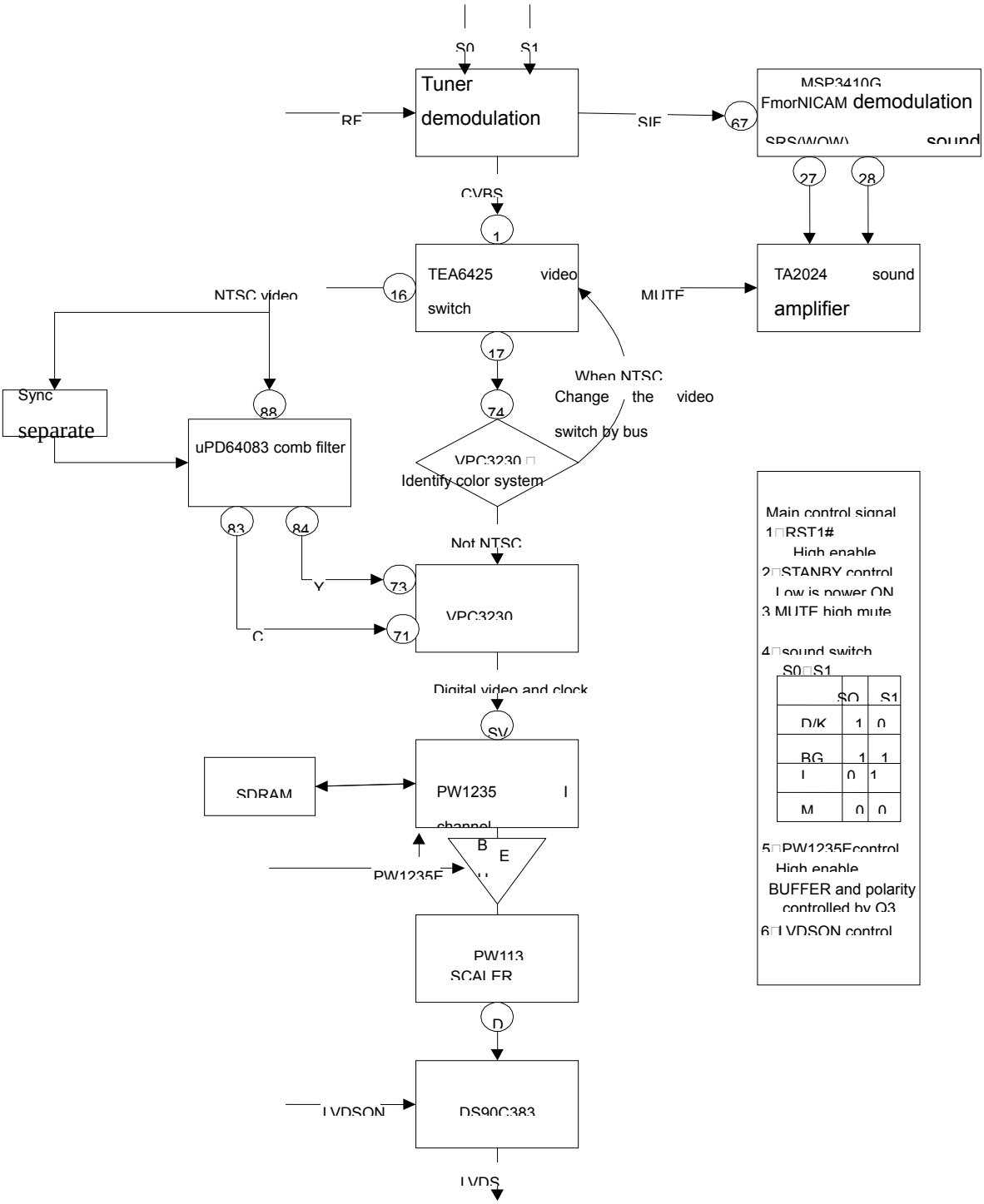
DVI interface 6□7pin is DDC data channel □U7□24LC21A□is an E^2ROM□which stores some DVI data parameter information □it connect to DDC data channel by bus□at the moment of power on □the status information is sent to host to identify□after identify□according to E^2ROM information outputs digital signal correctly□

VGA signal□video signal□DVI signal after digital disposal□sends to video format disposal ic PW113 to change the video format □ outputs the digital R,G,B signal which fits PDP display driver□

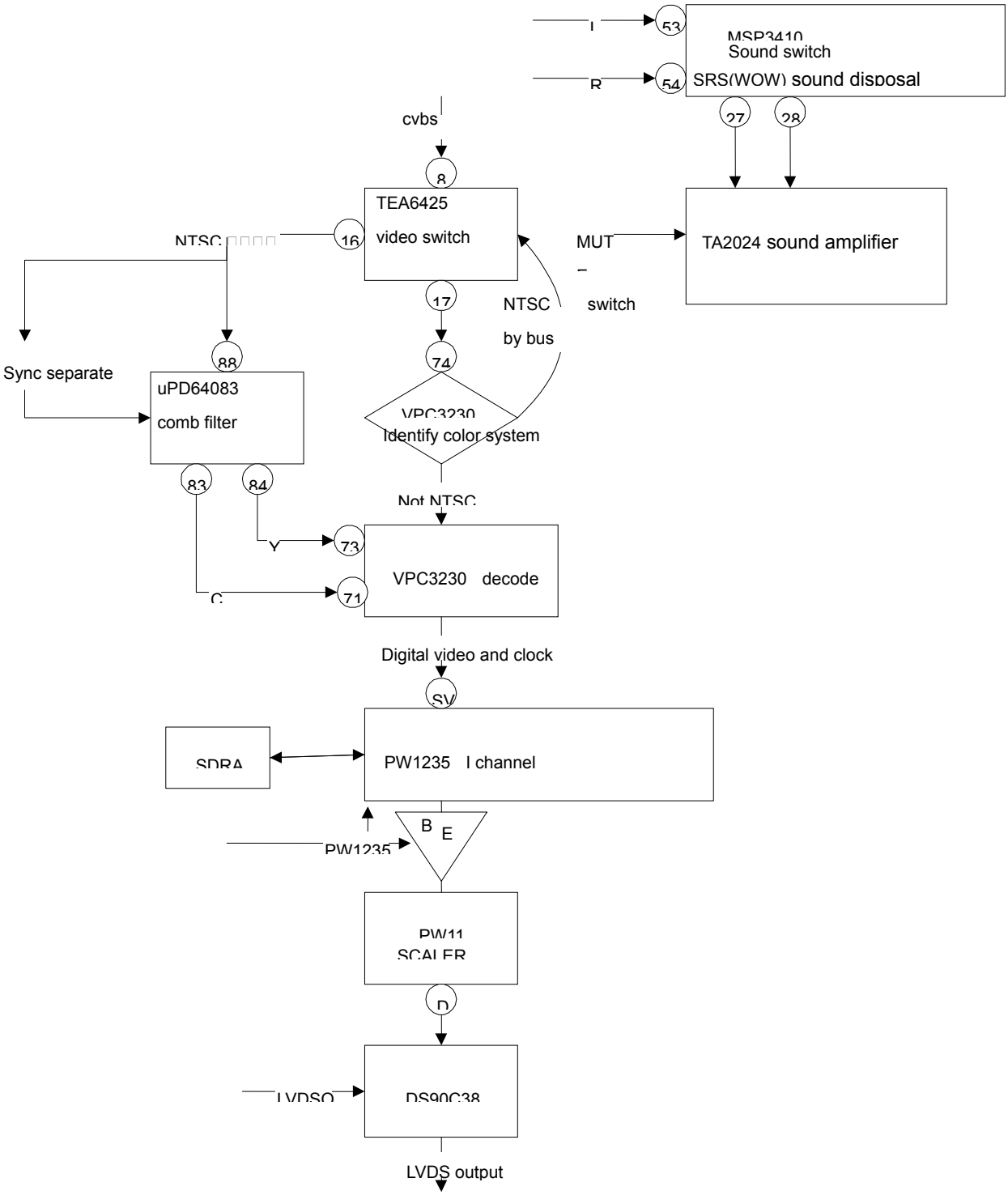
PW113 the input video signal after disposalled by PW113□outputs 852×480 resolution digital R,G,B signal which fits PDP panel spec and relevant sync□clock signal and transform them into LVDS by DS90CF383□send to PDP panel to control the panel display correctly□

3.2 each information flow

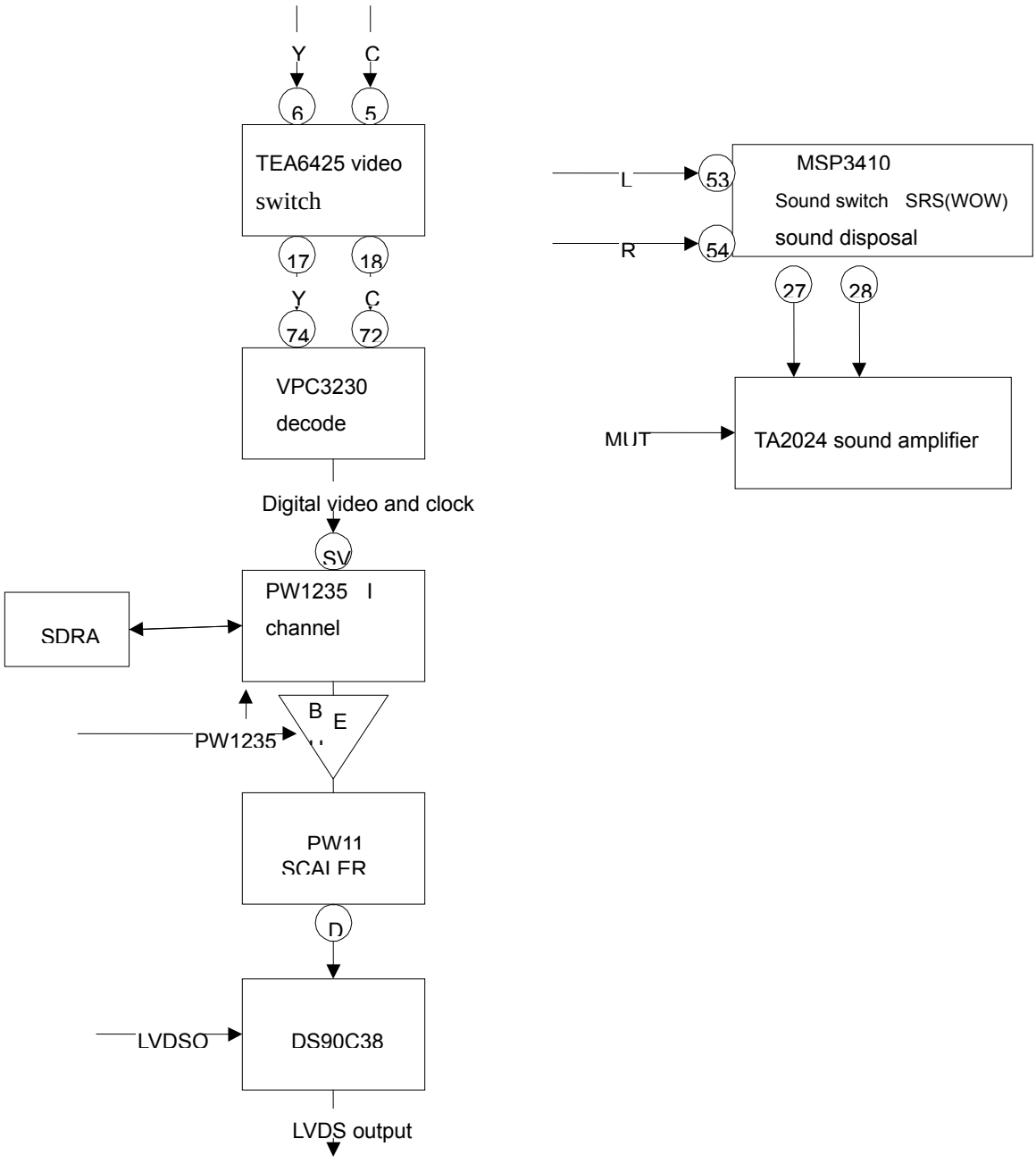
3.2.1 TV


S0
S1
Tuner
demodulation
RF
SIF
67
MSP3410G
FmorNICAM demodulation
SRS/WOW)
sound
27
28
CVBS
1
TEA6425 video
switch
16
NTSC video
MUTE
TA2024 sound
amplifier
17
When NTSC
Change the video
switch by bus
Sync
separate
88
74
uPD64083 comb filter
VPC3230
Identify color system
83
84
Not NTSC
Y
73
C
71
VPC3230
Digital video and clock
SV
SDRAM
PW1235 I
channel
B
E
PW1235E
PW113
SCALER
D
LVDSON
DS90C383
LVDS
Main control signal
1□RST1#
High enable
2□STANBY control
Low is power ON
3 MUTE high mute
4□sound switch
S0□S1
S0 S1
D/K 1 0
BG 1 1
I 0 1
M 0 0
5□PW1235Econtrol
High enable
BUFFER and polarity
controlled by Q3
6□LVDSON control

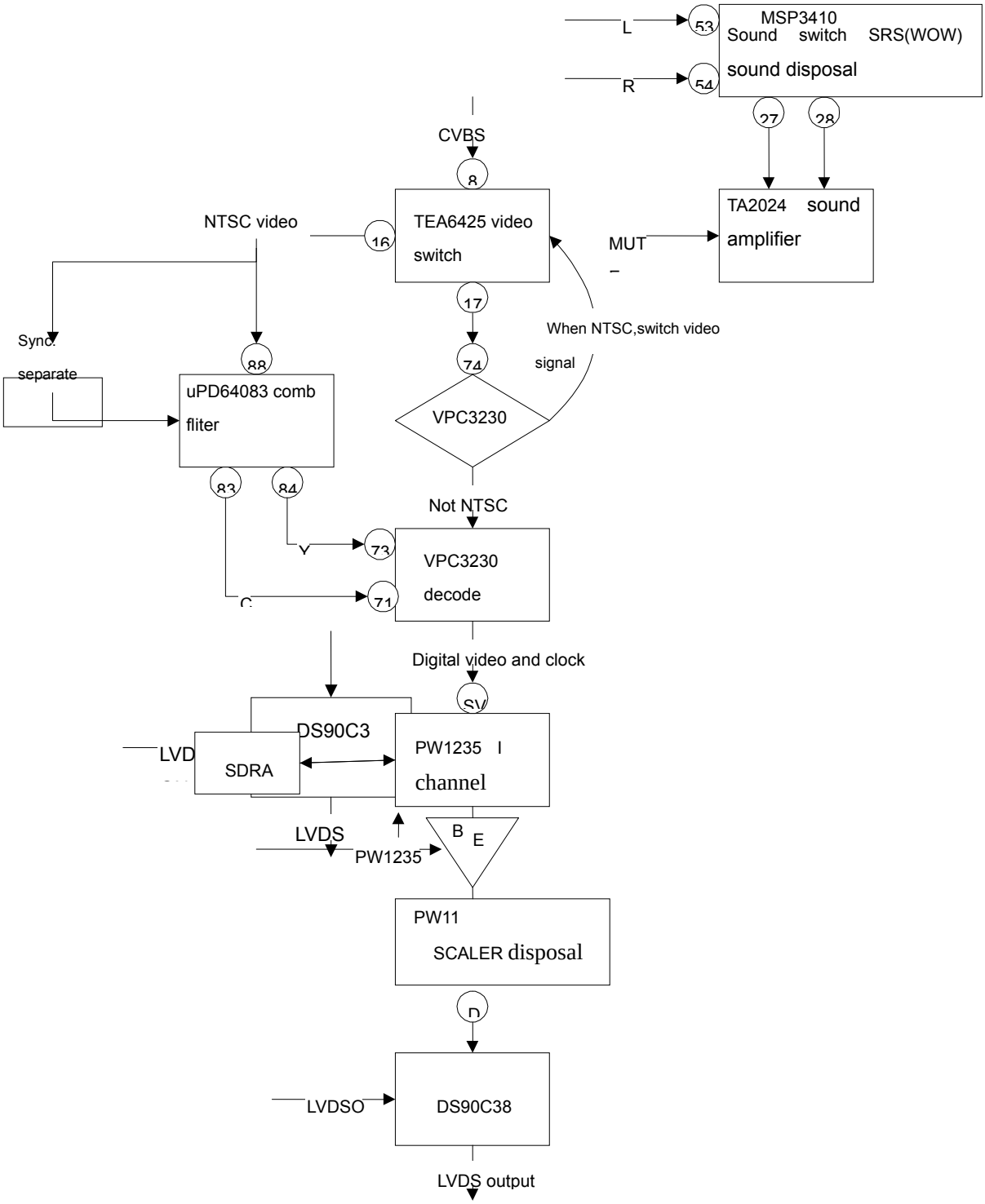
3.2.2 AV


MSP3410
Sound switch
SRS(WOW) sound disposal
cvbs
TEA6425
video switch
TA2024 sound amplifier
MUT
NTSC
switch
by bus
Sync separate
uPD64083
comb filter
Identify color system
Not NTSC
Y
C
VPC3230 decode
Digital video and clock
SDRA
PW1235 I channel
PW1235
B E
SCALER
LVDS output

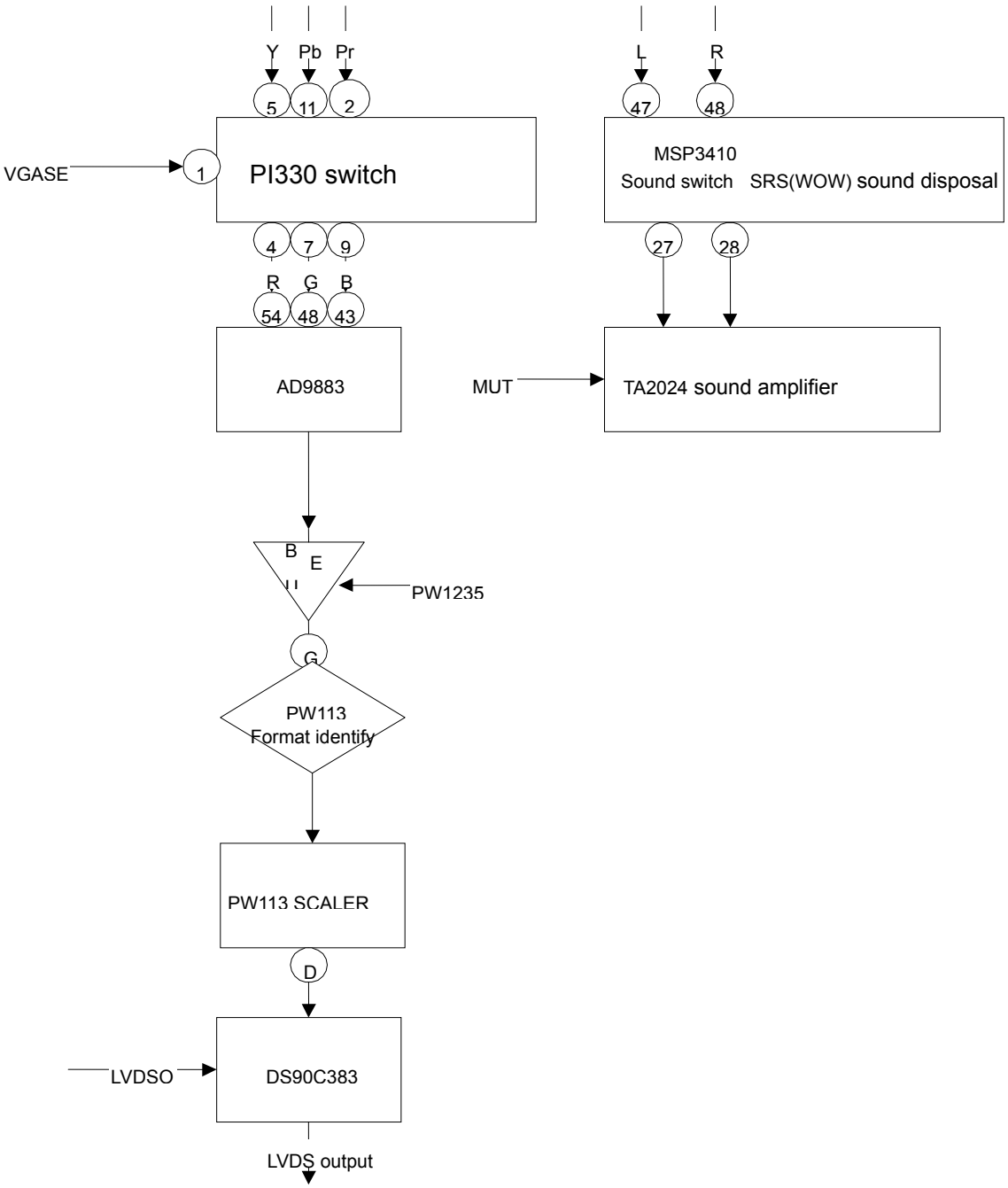
3.2.3 S-VIDEO


Y
C
6
5
TEA6425 video switch
17
18
Y
C
74
72
VPC3230 decode
Digital video and clock
SV
PW1235 I channel
SDRA
B
E
PW1235
PW11
SCALER
D
LVDSO
DS90C38
LVDS output
L
53
MSP3410
Sound switch SRS(WOW)
sound disposal
R
54
27
28
MUT
TA2024 sound amplifier

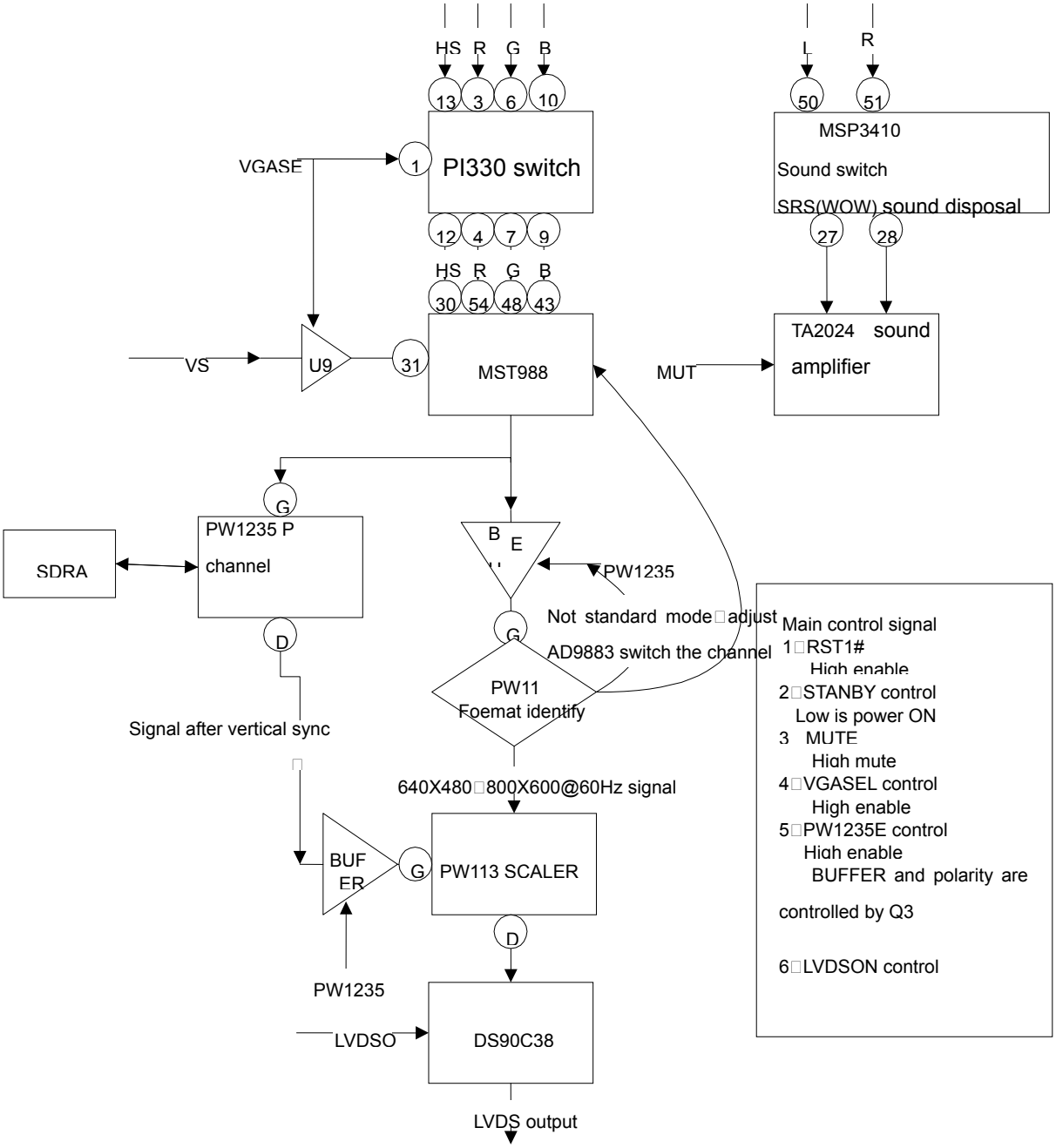
3.2.4 YcbCr


MSP3410
Sound switch SRS(WOW)
sound disposal
L
R
53
54
27
28
CVBS
8
TEA6425 video switch
16
NTSC video
MUT
–
TA2024 sound amplifier
17
When NTSC,switch video signal
74
VPC3230
Sync separate
88
uPD64083 comb fliter
83
84
Not NTSC
73
71
VPC3230 decode
Digital video and clock
SV
DS90C3
LVD
SDRA
PW1235 I channel
LVDS
PW1235
B E
PW11
SCALER disposal
D
LVDSO
DS90C38
LVDS output

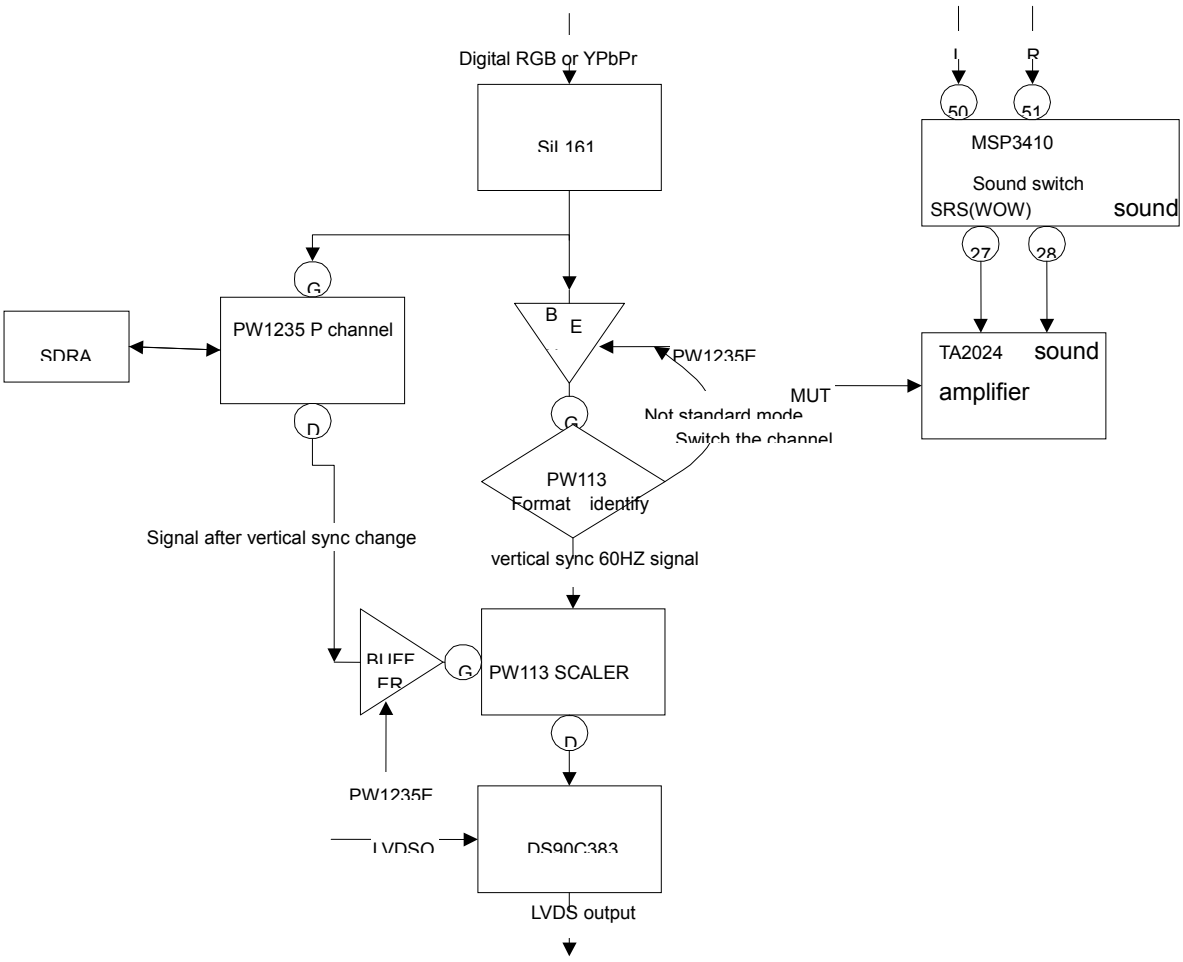
3.2.5 YpbPr


Y
Pb
Pr
5
11
2
L
R
47
48
VGASE
1
PI330 switch
MSP3410
Sound switch
SRS(WOW) sound disposal
4
7
9
27
28
R
G
B
54
48
43
AD9883
MUT
TA2024 sound amplifier
B
E
PW1235
G
PW113
Format identify
PW113 SCALER
D
LVDSO
DS90C383
LVDS output

3.2.6 VGA


HS R G B
13 3 6 10
L R
50 51
MSP3410
Sound switch
SRS(WOW) sound disposal
VGASE
1
PI330 switch
12 4 7 9
27 28
HS R G B
30 54 48 43
TA2024 sound amplifier
VS
U9
31
MST988
MUT
G
PW1235 P channel
SDRA
D
Signal after vertical sync
B E
PW1235
G
Not standard mode adjust
AD9883 switch the channel
PW11
Foemat identify
Main control signal
1 RST1#
High enable
2 STANBY control
Low is power ON
3 MUTE
High mute
4 VGASEL control
High enable
5 PW1235E control
High enable
BUFFER and polarity are controlled by Q3
6 LVDSON control
640X480 800X600@60Hz signal
BUF ER
G
PW113 SCALER
D
PW1235
LVDSO
DS90C38
LVDS output

3.2.7 DVI



3.3□system control process□

After connect the AC power input (we use 3 pins power jack□the GND pin must ground well).first of all ,standby power works□signal mainboard takes 5V-ST power supply□ the powers of PW113 begin to work□LED turns red. Resetting after V18□V33 power is normal□ PW113 initializes the system□sends STANDBY□L□signal□which controls main power begins to work□other power VT9□VT5□AVCC□PVDD□AVDD□OVCC□CVCC□PVCC□DAVCC□AVDD□ AVCC□DVDA□PVDD also work normally.MST9885□VPC3230□SiI161B□DS90CF383 take proper power supply. Moreover LED signal control LED to turn yellow and glitter□it is said that it controls normally □At last LVDSON signal from 43pin of PW113is high□it let DS90CF383 begin to work□After this it is in normal work state□input source is last time source before power off□

3.3.1□when choice VGA mode by remote device □PW113 controls MST9885 by I^2C bus□enable SiI161B and VPC3230□let them work in low consume mode□which can save power and reduce interfere□At the moment VGASEL signal from PW113 output parks VGA input channel in PI5V330. If VGA signal inputs, MST9885 outputs Horizontal and Vertical Sync signal and data signal□and send to PW113□which outputs format commutation data . After DS90CF383(DS transmitter)□it transforms to the signal fitting the PDP panel demand□ because SiI161B□DS90CF383 both in normal work state□when DVI signal inputs, display video□if no VGA signal□MST9885 can not output digital Horizontal and Vertical Sync signal □after examined by PW113,displays pc icon on the left and top of PDP panel □other part display black. If no input after 60 sec, it hints to enter "save power mode" □At the moment , MST9885 in normal work state□examines VGA signal ceaselessly□so it can arouse automatically in VGA mode. It is said that when VGA signal inputs, it can work normally from standby state□

3.3.2□when in TV□AV□YCbCr mode by remote device□PW113 controls VPC3230 by I^2Cbus□otherwise PW113 controls MST9885 on the fly □output in high impedance state□by I^2Cbus.Because tuner N901□VPC3230□ DS90CF383 all in normal work state□when video signal inputs□PDP panel display normally□if no video signal input□under the control of PW113□PDP panel displays blue background□if no signal 15 mins□power off automatically and into standby state. It can not arouse automatically□

3.3.3□When in DVI(digital RGB) mode by remote device□PW113 controls SiI161B□and enables VPC3230□and let it working in low consume mode□otherwise PW113 controls MST9885 on the fly□output in high impedance state□by I^2C bus□because SiI161B□DS90CF383 both in normal work state□when DVI signal inputs, display video□if no DVI signal□SiI161B do not output digital Horizontal and Vertical Sync signal □after examined by PW113,displays DVI icon on the left and top of PDP panel □other part display black. If no input after 60 sec, it hints to enter "save power mode"work state□At the moment ,SiI161B in normal work state□ examines DVI signal ceaselessly□so it can arouse automatically in DVI mode. It is said that when DVI signal inputs, it can work normally from standby state□

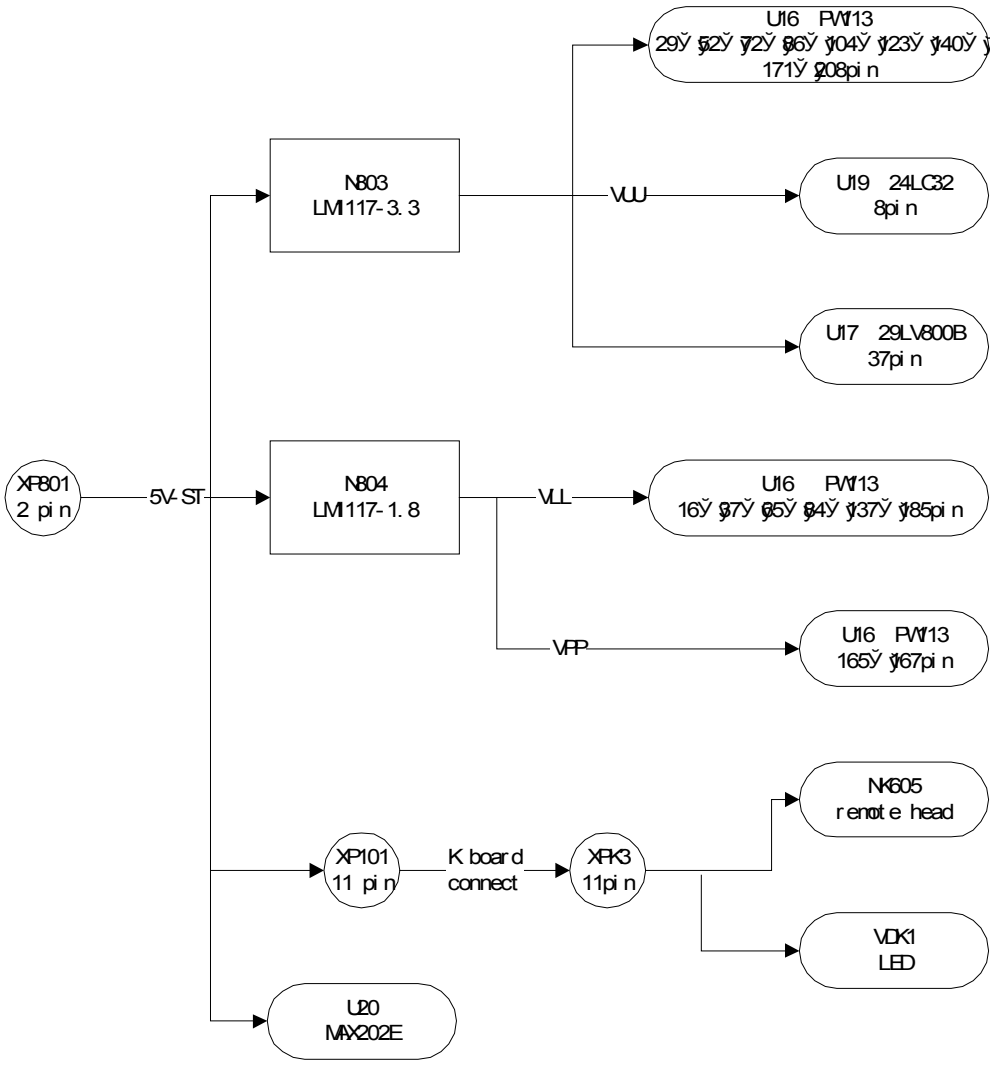
3.4□power supply system□

3.4.1□main power supply

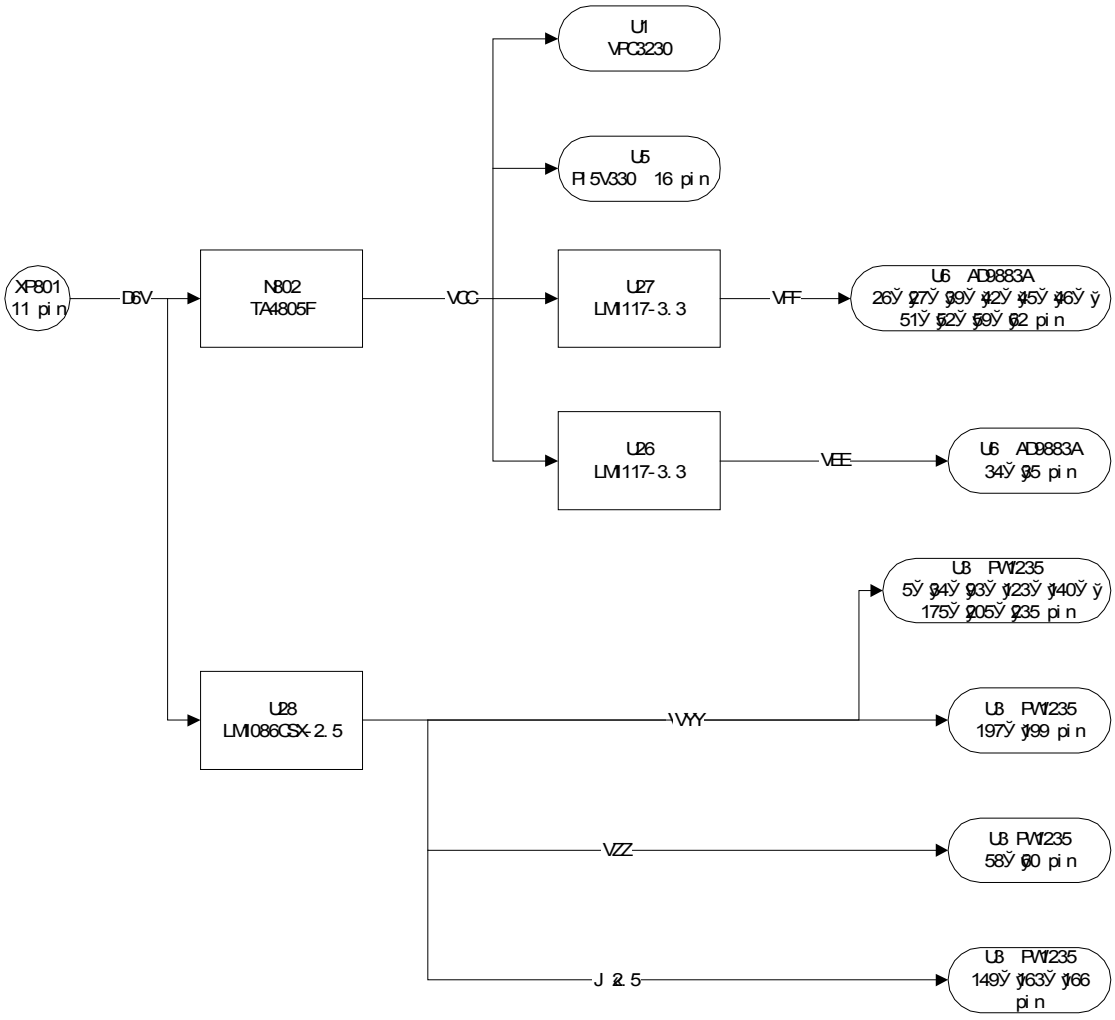
D6V□steady voltage to 5V supply for VPV3230□AD9883 analog power□5V-ST□standby power□to PW113□AM29LV800BT□ROM□□24LC32□MAX202E□VDD(3.3V)□VPC3230□ MST9885□DS90CF383 power□+32V□RF tuner tuning power□A6V□steady voltage to Av board 5V etc. □A12V□steady voltage to AV board 8V etc.□12VAMP□sound amplifier TA2024 power□

3.4.2 main power form and power branch□

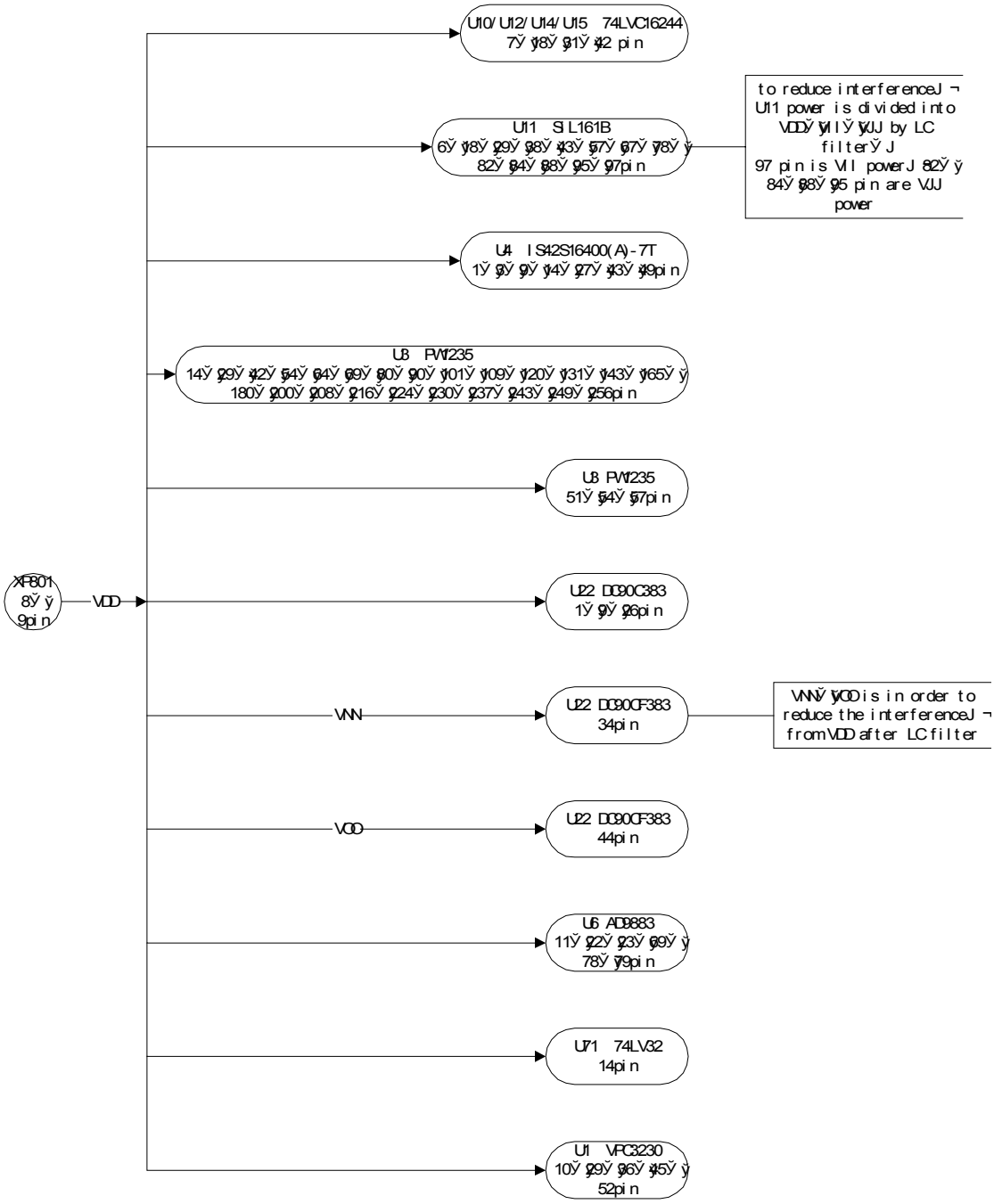
3.4.2.1 5V-STpower branch



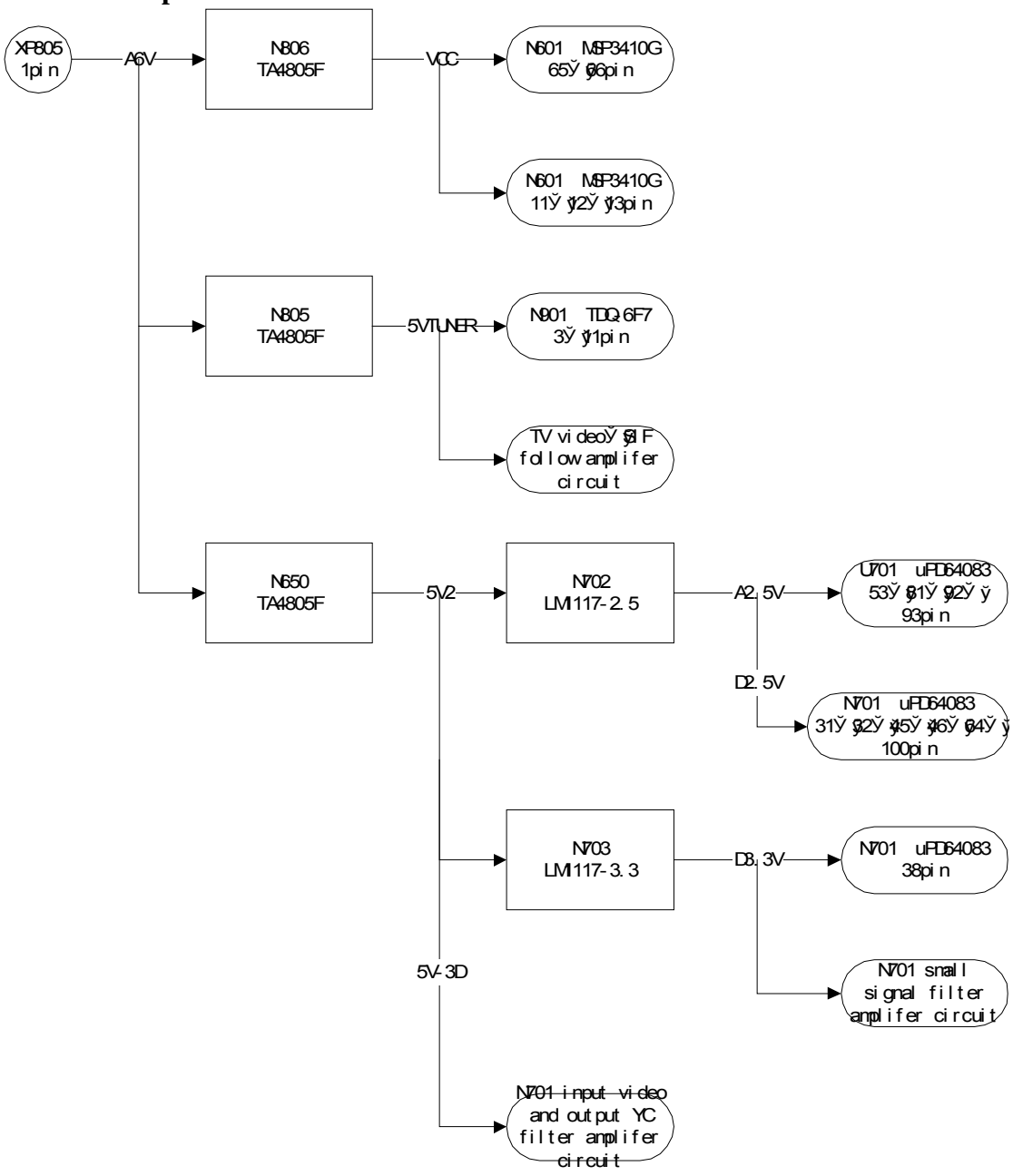
3.4.2.2 D6V power branch


U1
VPC3230
U5
PI5V330 16 pin
XP801
11 pin
D5V
N802
TA4805F
VCC
U27
LM1117-3.3
VFF
U6 AD9883A
26Ÿ 27Ÿ 39Ÿ 42Ÿ 45Ÿ 46Ÿ
51Ÿ 52Ÿ 59Ÿ 62 pin
U26
LM1117-3.3
VEE
U6 AD9883A
34Ÿ 35 pin
U3 PW1235
5Ÿ 34Ÿ 43Ÿ 123Ÿ 140Ÿ
175Ÿ 205Ÿ 235 pin
U28
LM1086CSX-2.5
VYY
U3 PW1235
197Ÿ 199 pin
VZZ
U3 PW1235
58Ÿ 60 pin
J 2.5
U3 PW1235
149Ÿ 163Ÿ 166
pin

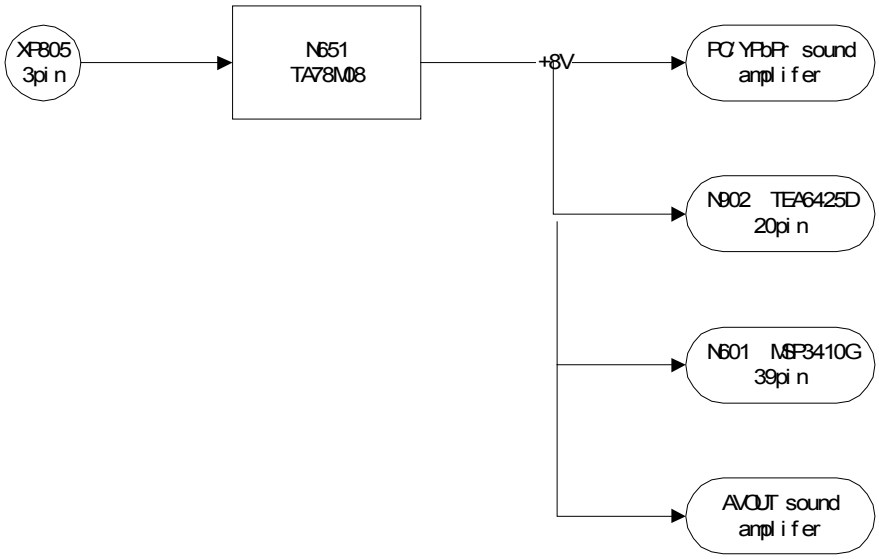
3.4.2.3 VDD(3.3V) power branch



3.4.2.4 A6Vpower branch

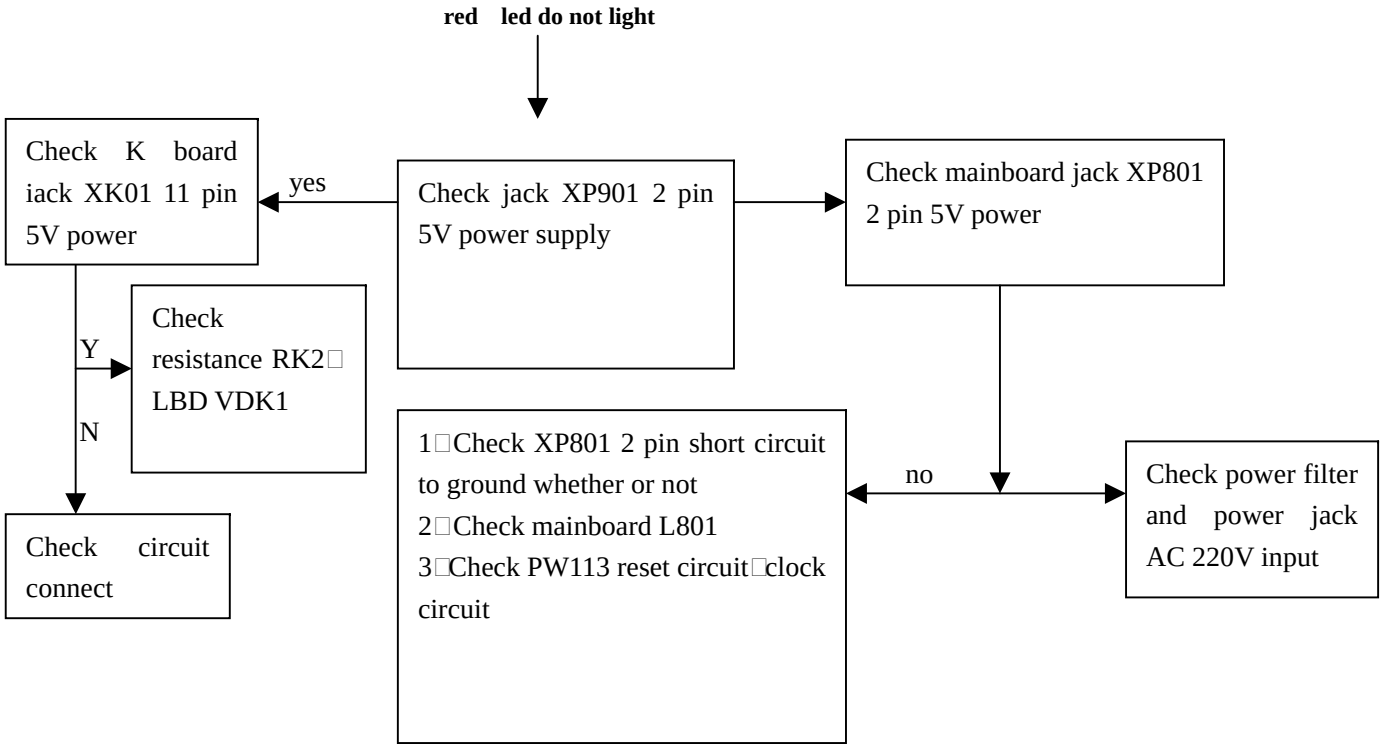


3.4.2.5 A12Vpower branch

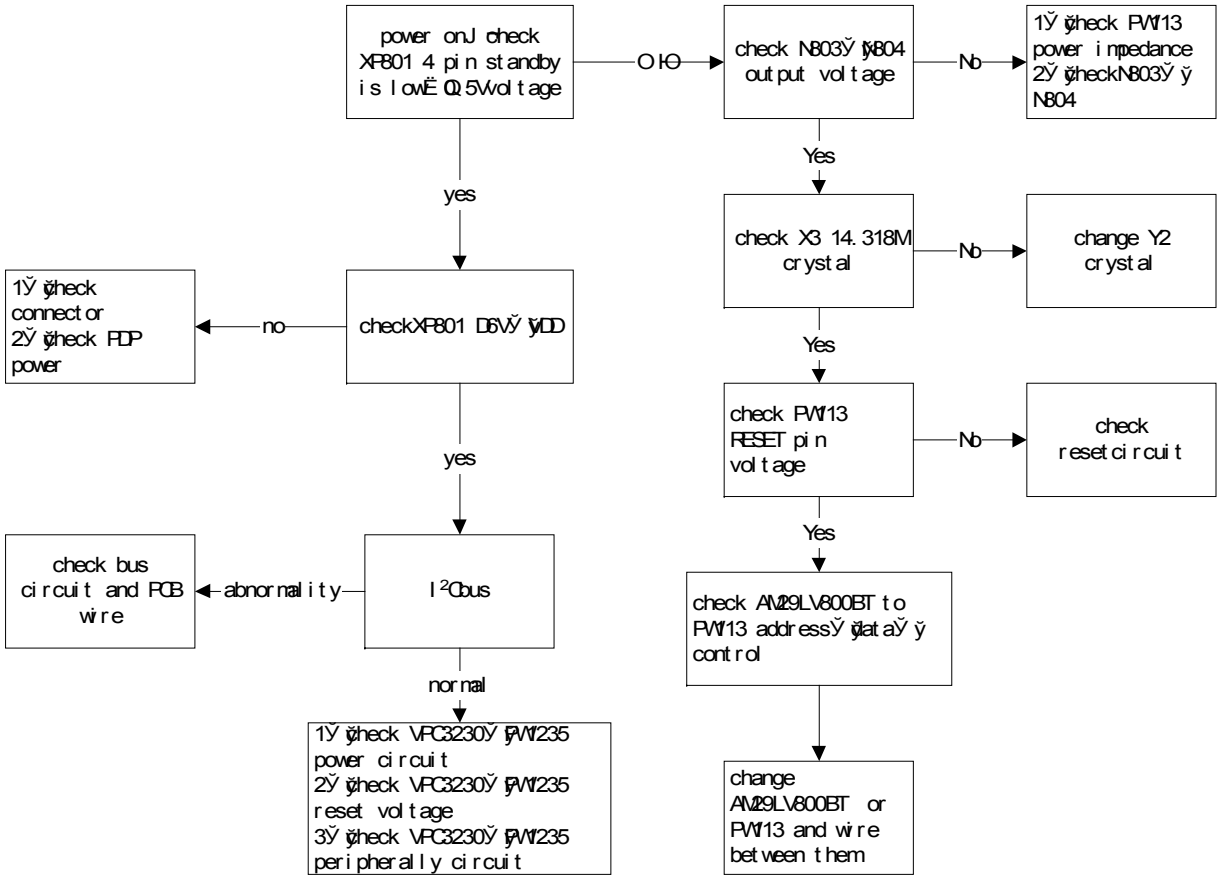


Part :Typical Defectives and Repair of PT4206

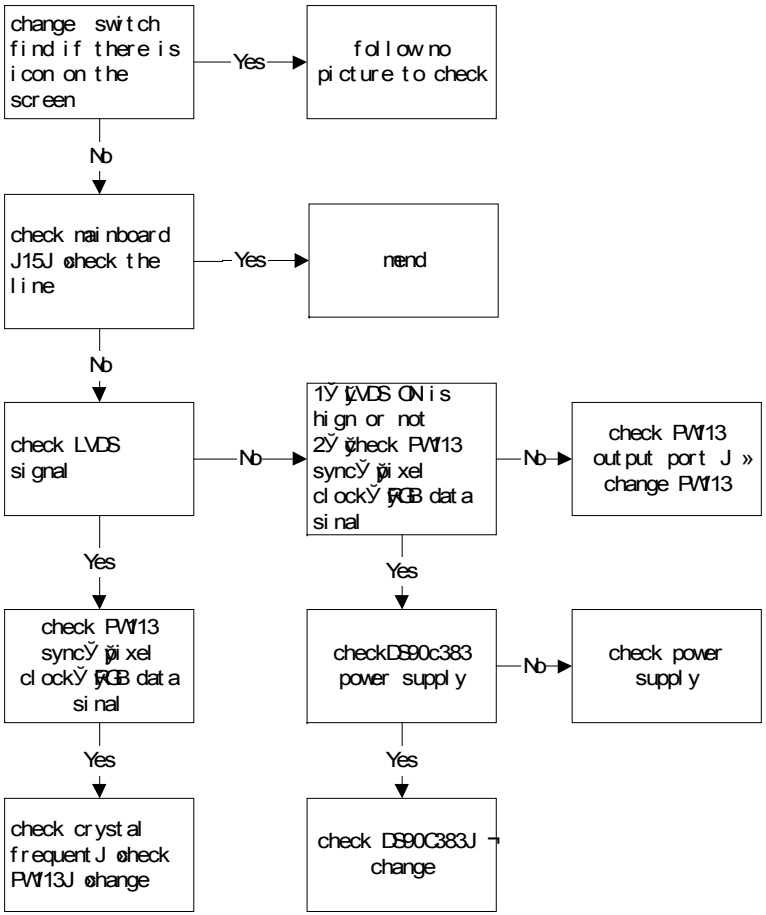
one red led do not light



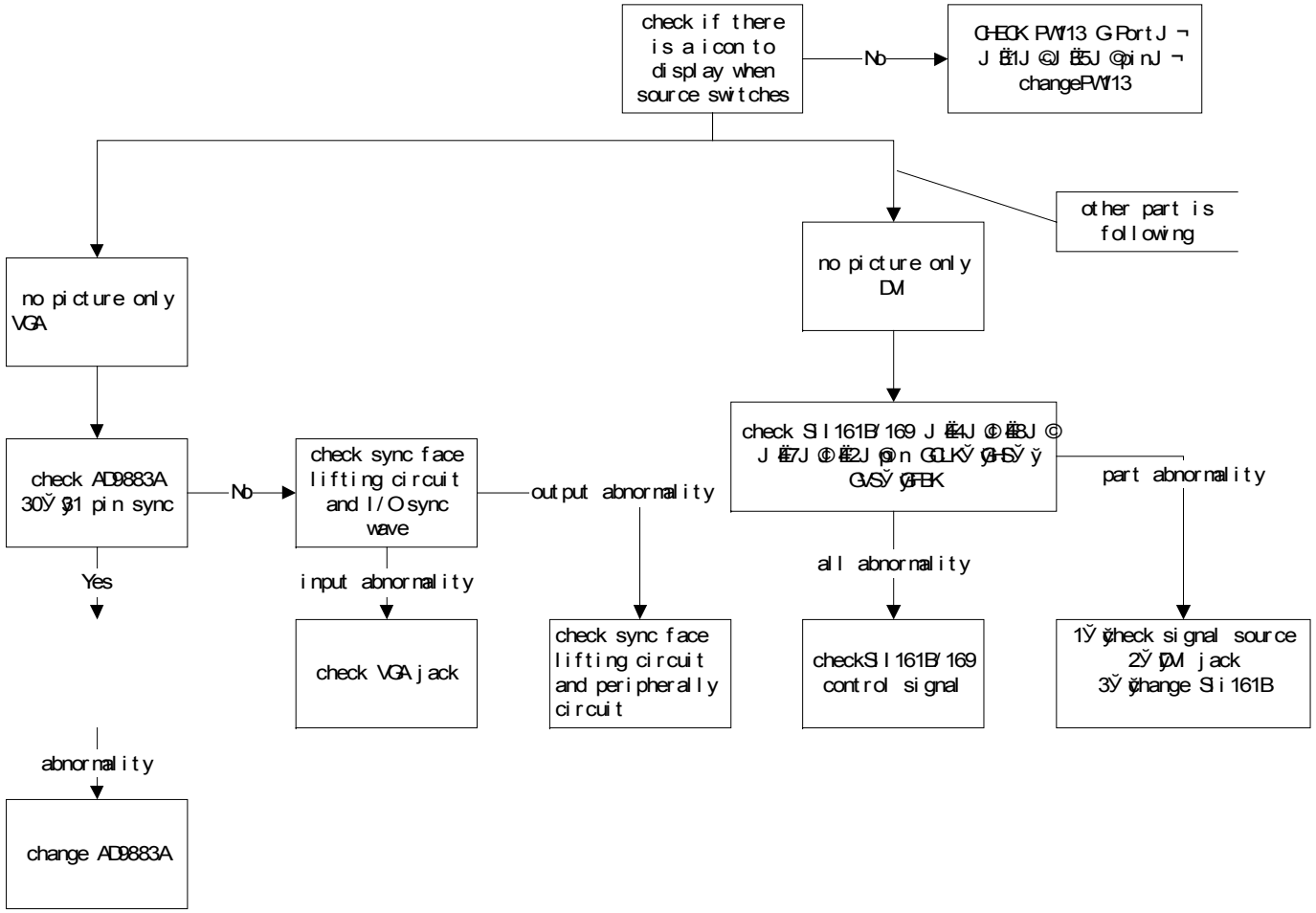
two The red led lights but doesn't turn to yellow after power on and black display

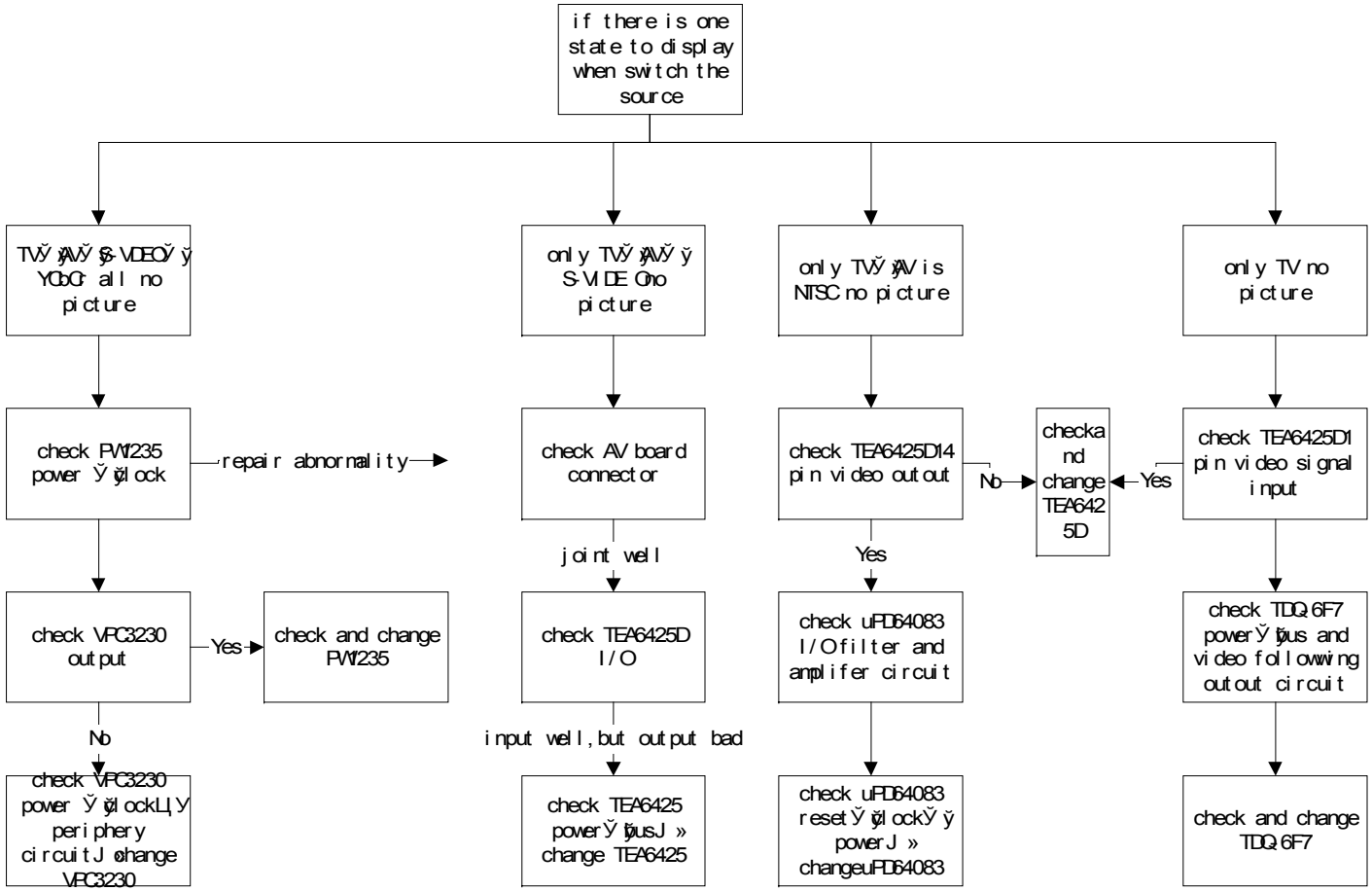


three The red led light but turn to other color after power on and black display

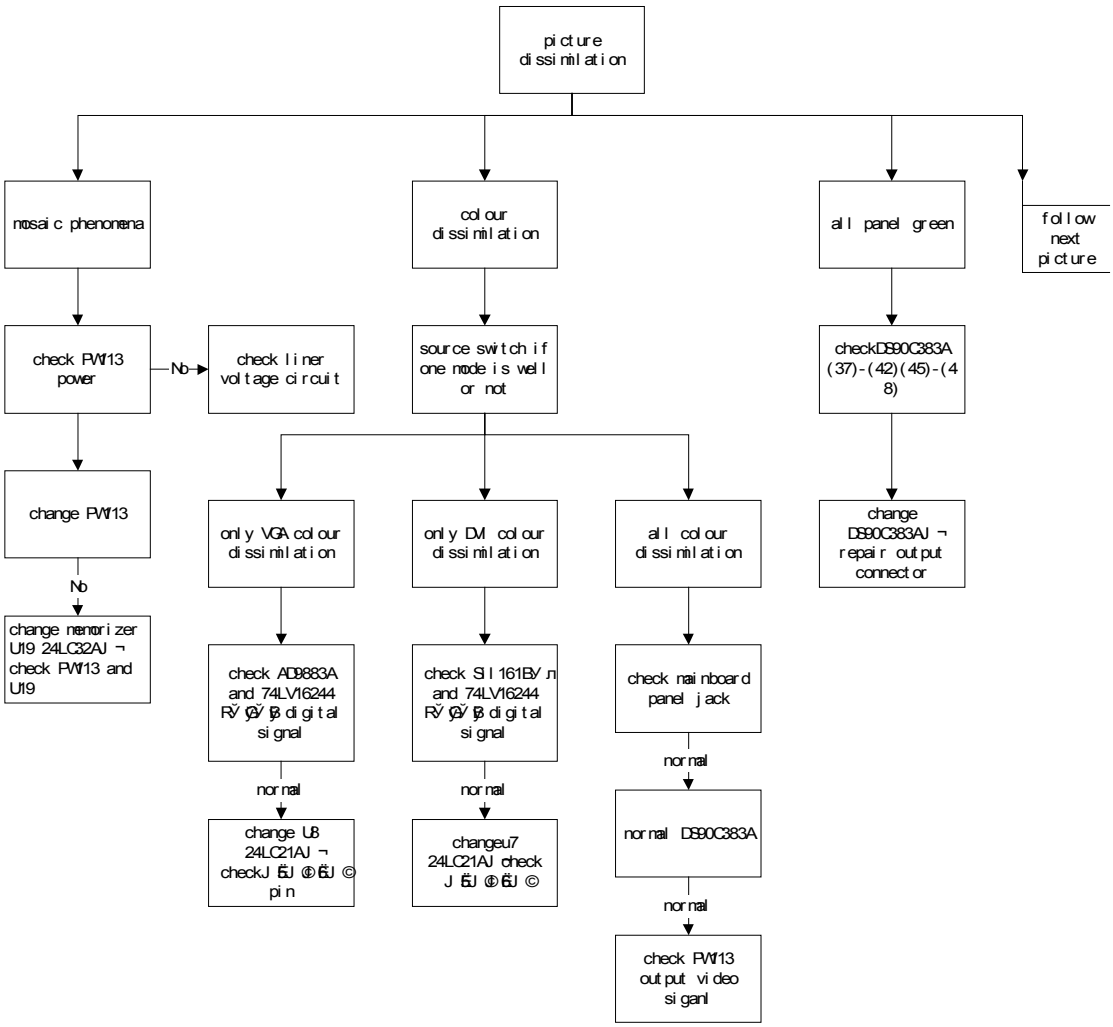


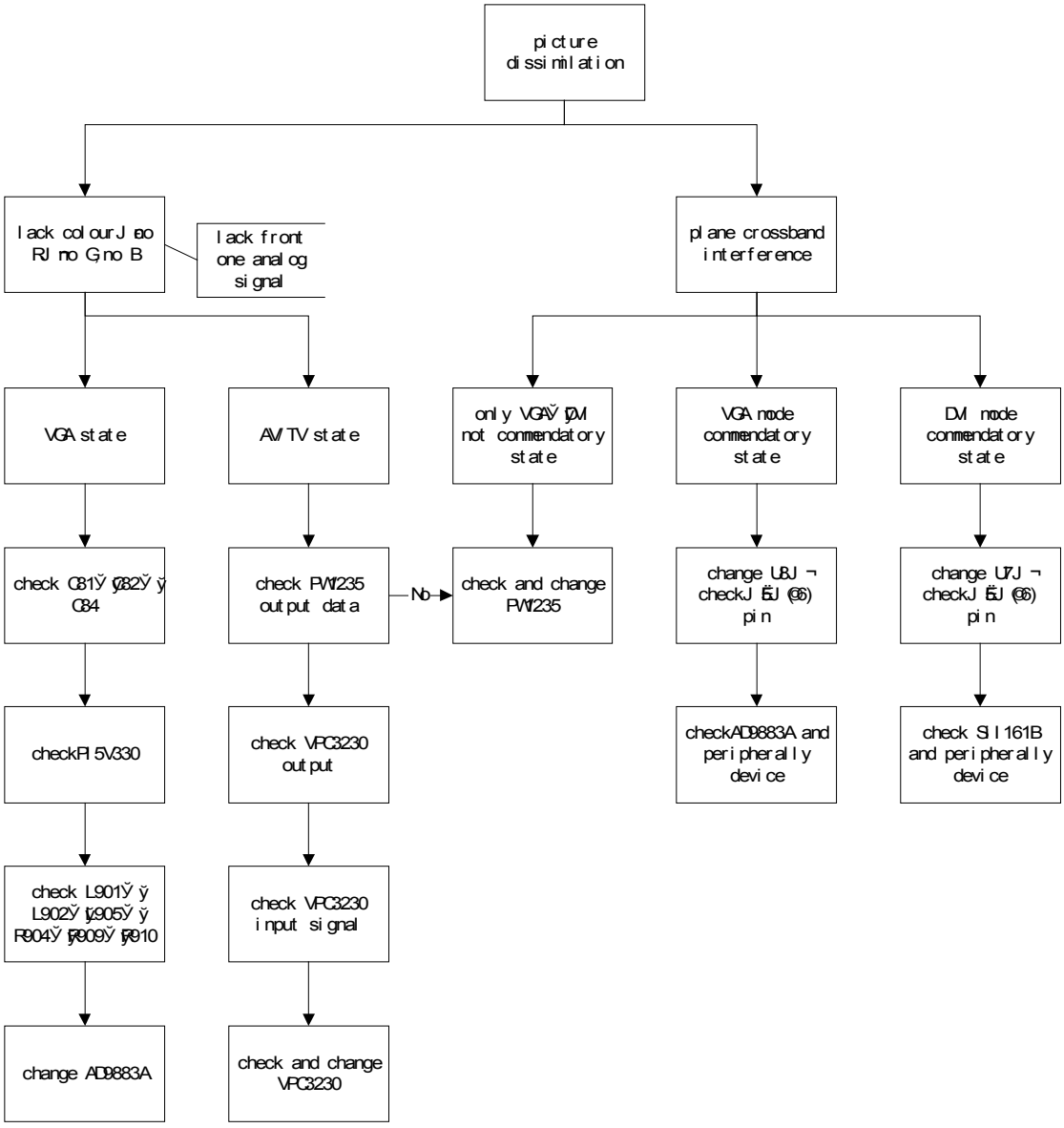
four no picture



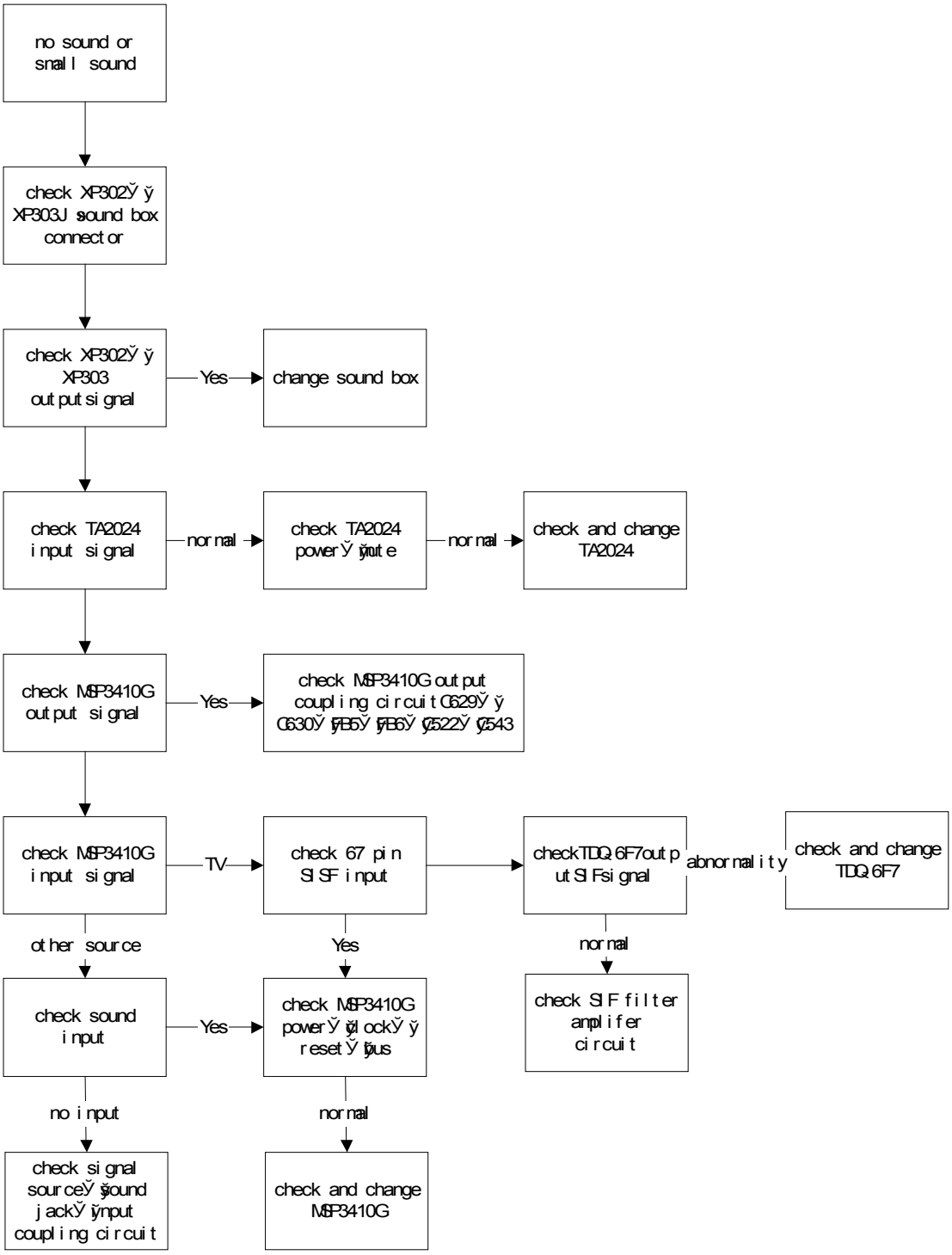

if there is one state to display when switch the source
TV AV S-VIDEO YCbCr all no picture
only TV AV S-VIDEO no picture
only TV AV is NTSC no picture
only TV no picture
check PW1235 power lock
repair abnormality
check AV board connector
check TEA6425D14 pin video outout
No
Yes
check and change TEA6425D
check TEA6425D1 pin video signal input
joint well
Yes
check VPC3230 output
Yes
check and change PW1235
check TEA6425D I/O
check uPD64083 I/O filter and amplifer circuit
check TDQ6F7 power bus and video followwing outout circuit
No
input well, but output bad
check VPC3230 power lock L Y periphery circuit J change VPC3230
check TEA6425 power bus J » change TEA6425
check uPD64083 reset lock power J » changeuPD64083
check and change TDQ6F7

Five picture dissimilation

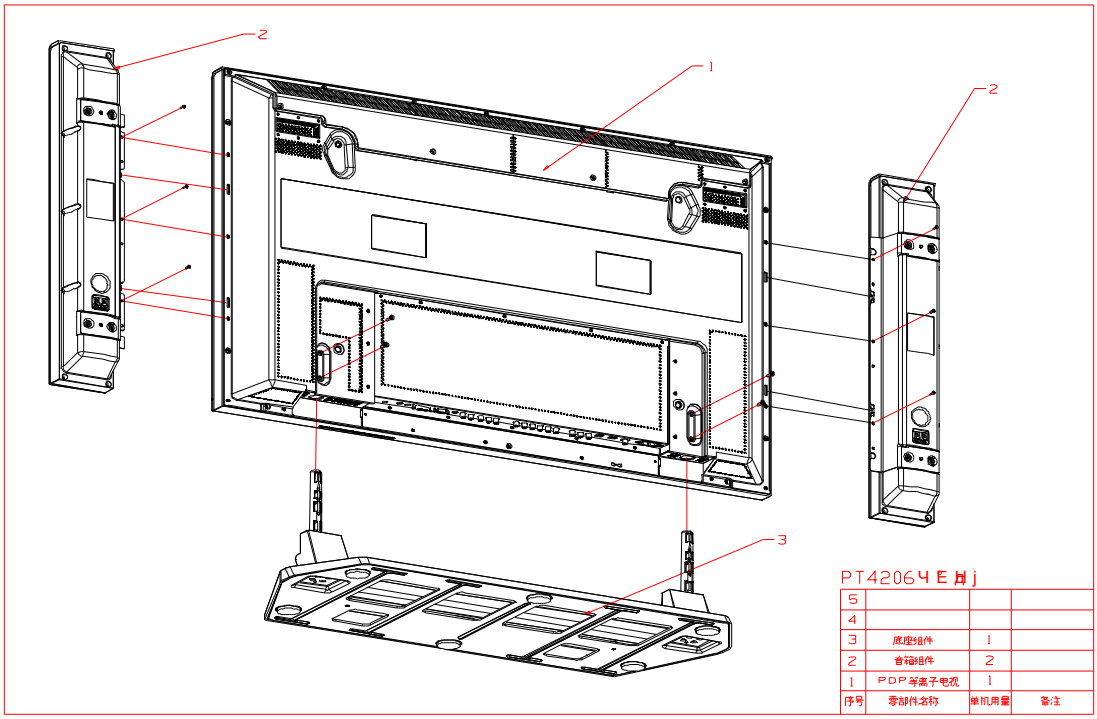



picture dissimilation
lack colour Jno RJ no G,no B
lack front one analog signal
plane crossband interference
VGA state
AV/TV state
only VGAŸ DVI not commendatory state
VGA mode commendatory state
DVI mode commendatory state
check C81Ÿ ÿ C82Ÿ ÿ C84
check PVI1235 output data
No
check and change PVI1235
change U8J ¬ checkJ ßJ (36) pin
change U7J ¬ checkJ ßJ (36) pin
checkFl5V330
check VPC3230 output
checkADI9883A and peripherally device
check SII161B and peripherally device
check L901Ÿ ÿ L902Ÿ ÿ L905Ÿ ÿ R904Ÿ ÿ R909Ÿ ÿ R910
check VPC3230 input signal
change ADI9883A
check and change VPC3230

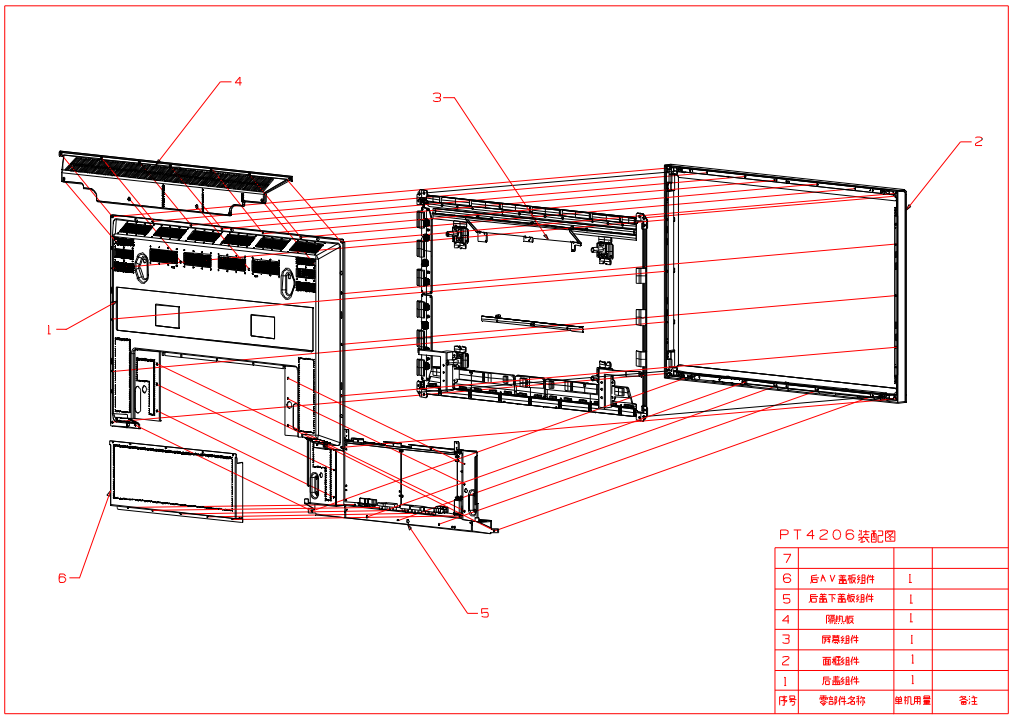
six no sound or small sound

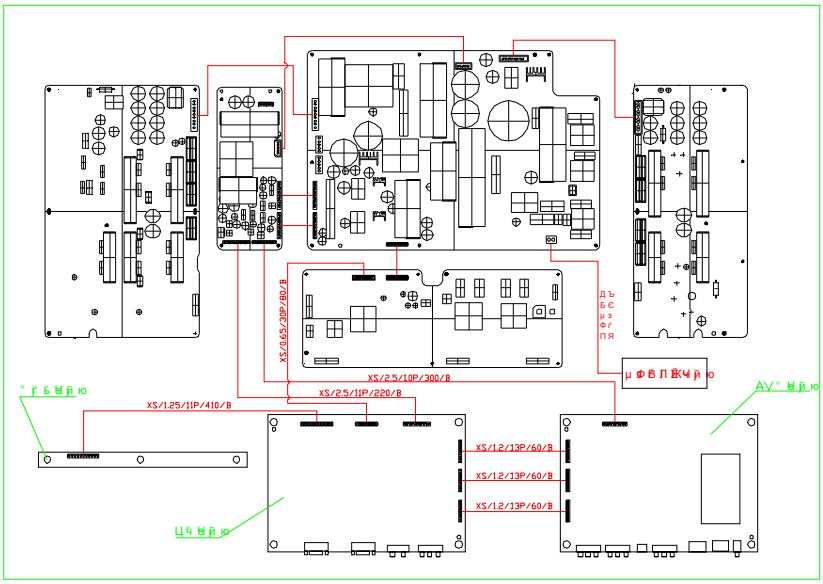


Annex 1


2
1
2
3
PT42064 E Hj
5
4
3 底座组件 1
2 音箱组件 2
1 PDP等离子电视 1
序号 零部件名称 单机用量 备注

Annex 2


4
3
2
1
6
5
PT4206装配图
7
6 后AV盖板组件 1
5 后盖下盖板组件 1
4 隔机板 1
3 屏幕组件 1
2 面框组件 1
1 后盖组件 1
序号 零部件名称 单机用量 备注


XS/0.65/30P/480/B
XS/2.5/10P/300/B
XS/2.5/11P/220/B
XS/1.25/11P/410/B
XS/12/13P/60/B
XS/12/13P/60/B
XS/12/13P/60/B